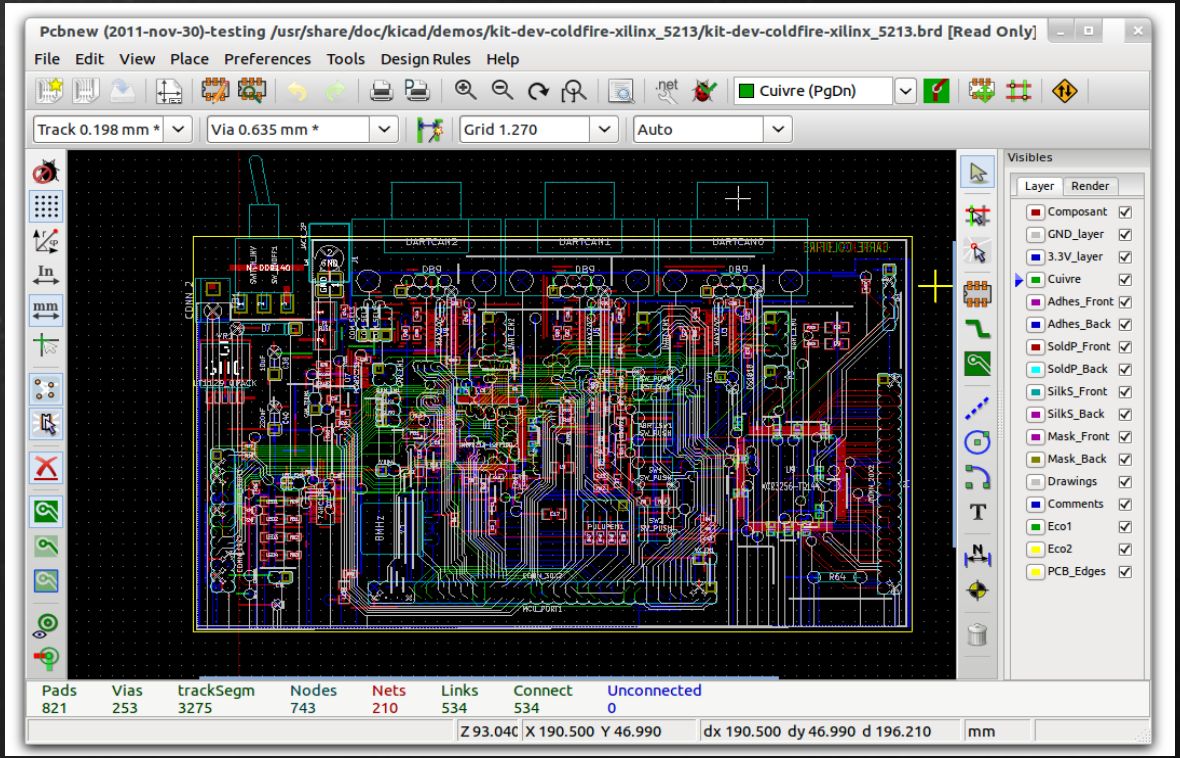
Release your hardware hacker potential with KiCAD

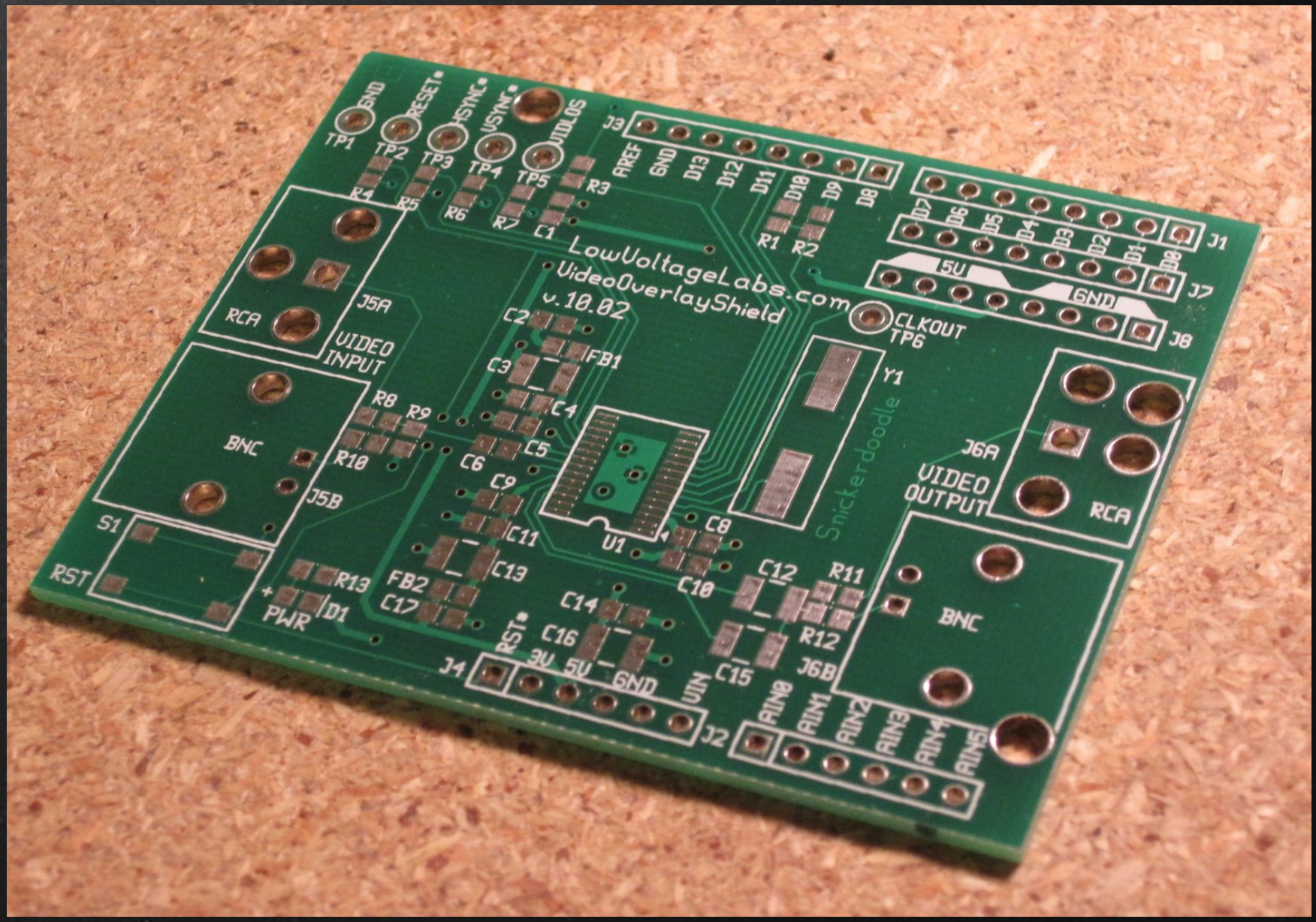


Eric Thompson
LowVoltageLabs.com

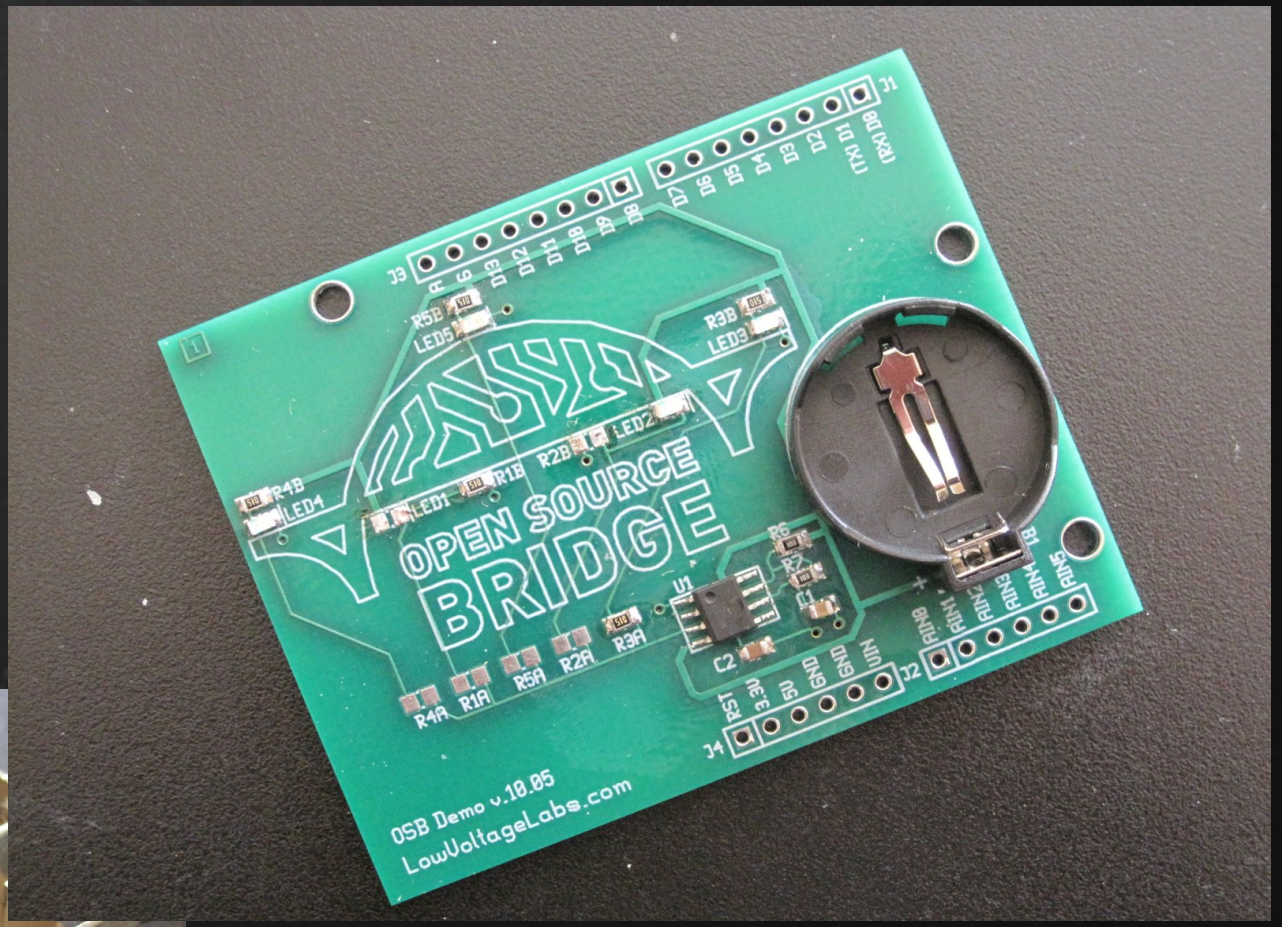
Create a board with KiCAD

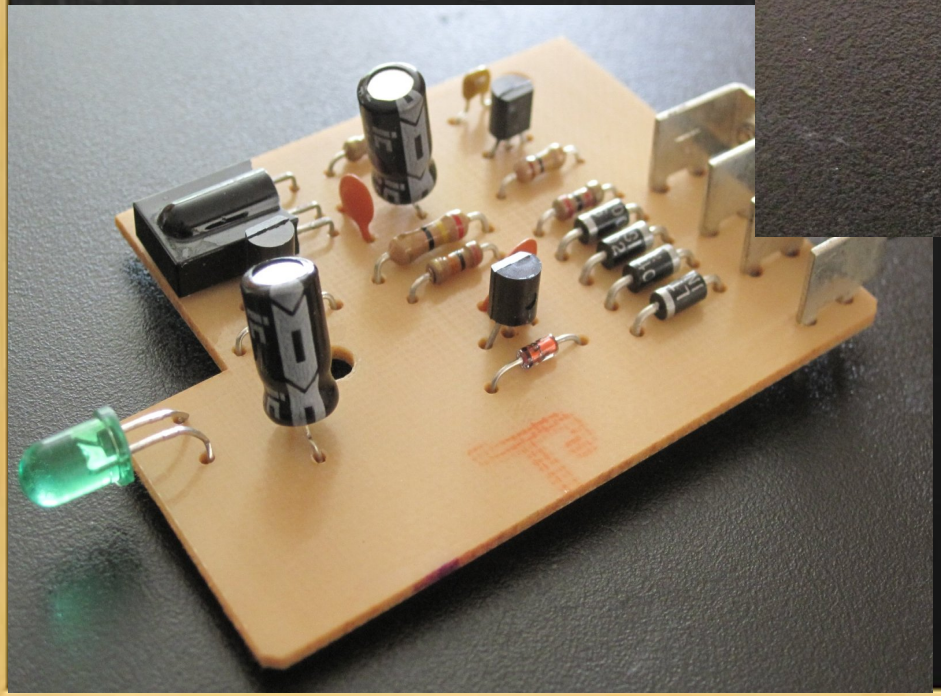
- What is a PCB?
- What is a KiCAD?
- Block diagram
- Schematic
- Schematic attribute editor
- Error check the schematic
- PCB layout
- Error check the layout
- Gerber files
- Build boards

What is a printed circuit board (PCB)?



What is a PCB made of?





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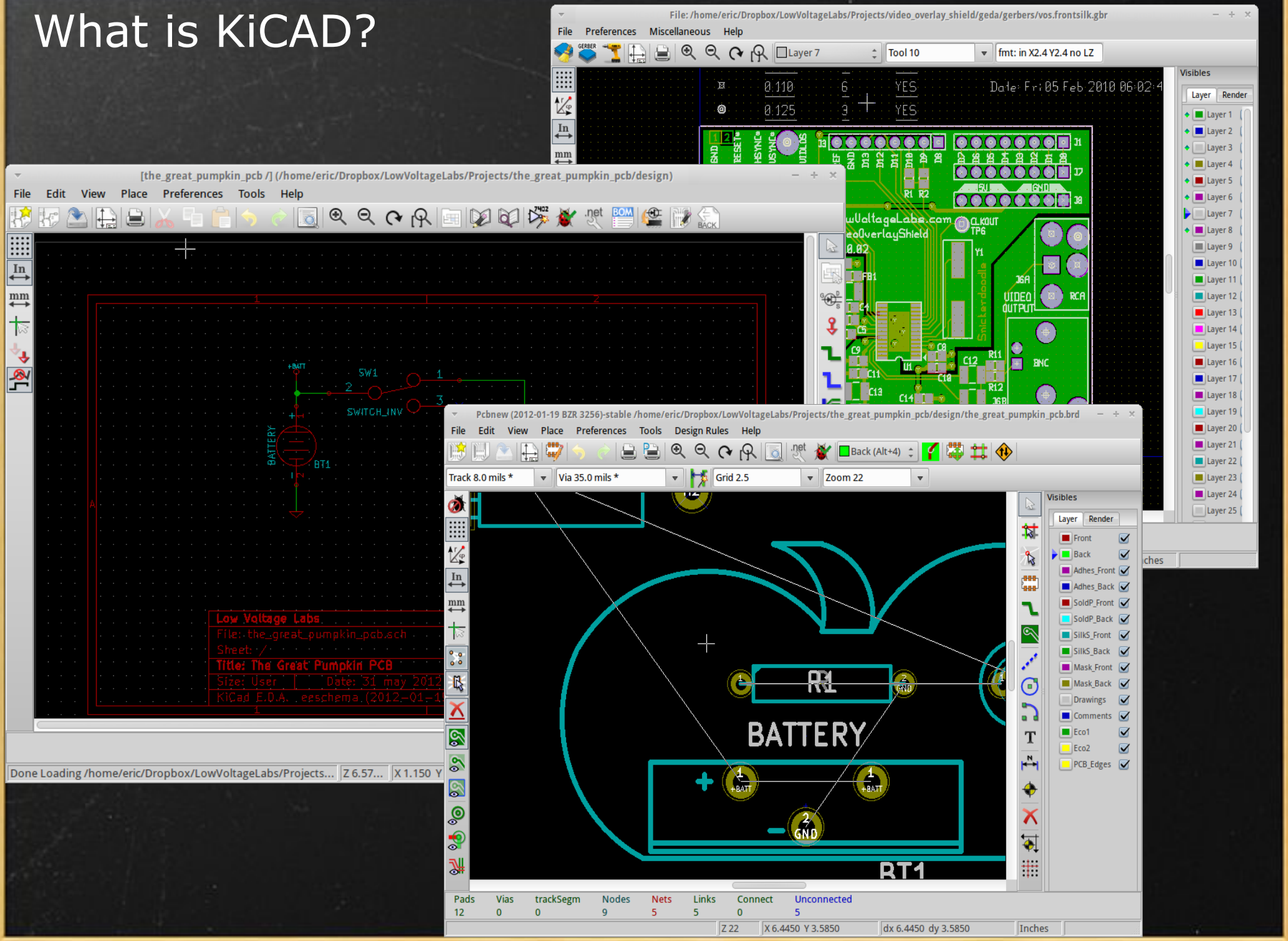
What is KiCAD?



KiCAD website -> http://www.kicad-pcb.org/

KiCad EDA Software Suite

http://www.kicad-pcb.org/

Press Tab to search KiCad EDA

Dashboard › Kicad EDA › KiCad EDA Software Suite

Browse Log In Search Confluence

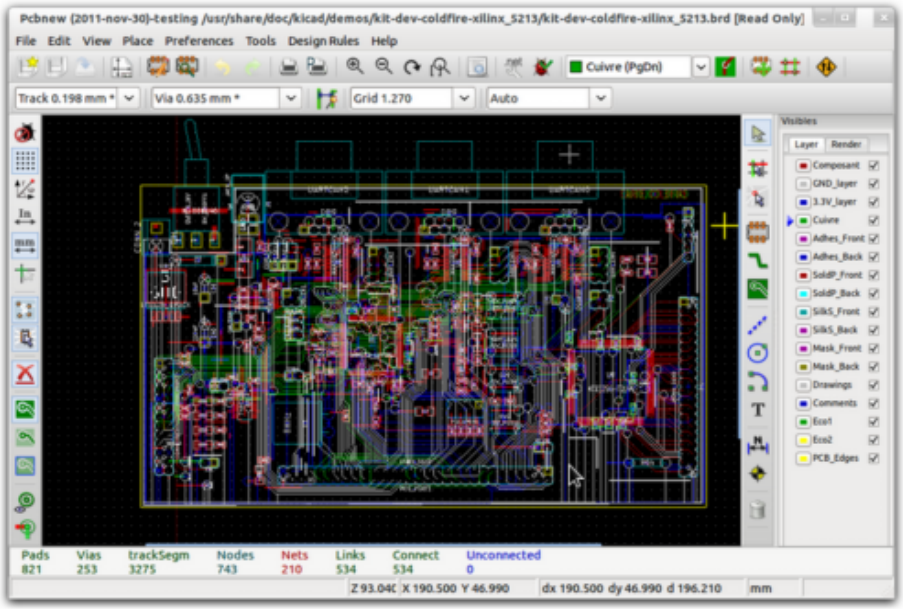
Search

- KiCad EDA Software Suite
  - About KiCad
  - Download Kicad
  - File Formats
  - Frequently Asked Questions
  - KiCad Documentation
  - Platforms
  - Video Tutorials

Tools

KiCad EDA Software Suite

KiCad is an EDA software suite for the creation of professional schematics and printed circuit boards. Kicad runs on Windows, Linux and Apple OS X and is released under the open-source GNU GPL v2.



Use KiCad

Download KiCad

Build KiCad

Documentation

Frequently Asked Questions

Kicad user mailing list

Videos & Tutorials

About KiCad

Contribute to KiCad

Developer Space (join us!)

Localization

Report a Bug

Others Links

News

Press

IRC for kicad

Launchpad, sourceforge, Fm, oh loh

Install KiCad

The easiest way to install KiCad and its documentation on Linux is via a PPA link like the one available from the Adam Wolf page:

```
sudo add-apt-repository ppa:adamwolf/kicad-testing-daily
sudo apt-get update
sudo apt-get install kicad kicad-doc-en
```

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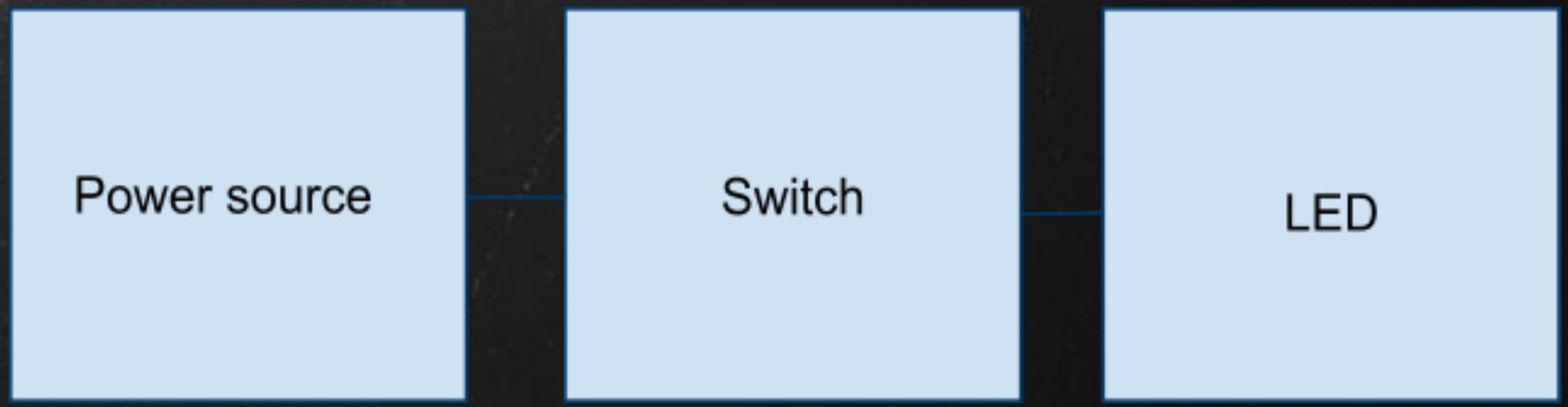
Idea:
Create a PCB for the flickering LEDs available from the Evil Mad Science shop.
http://www.evilmadscientist.com/article.php/simplepumpkins

Block diagram



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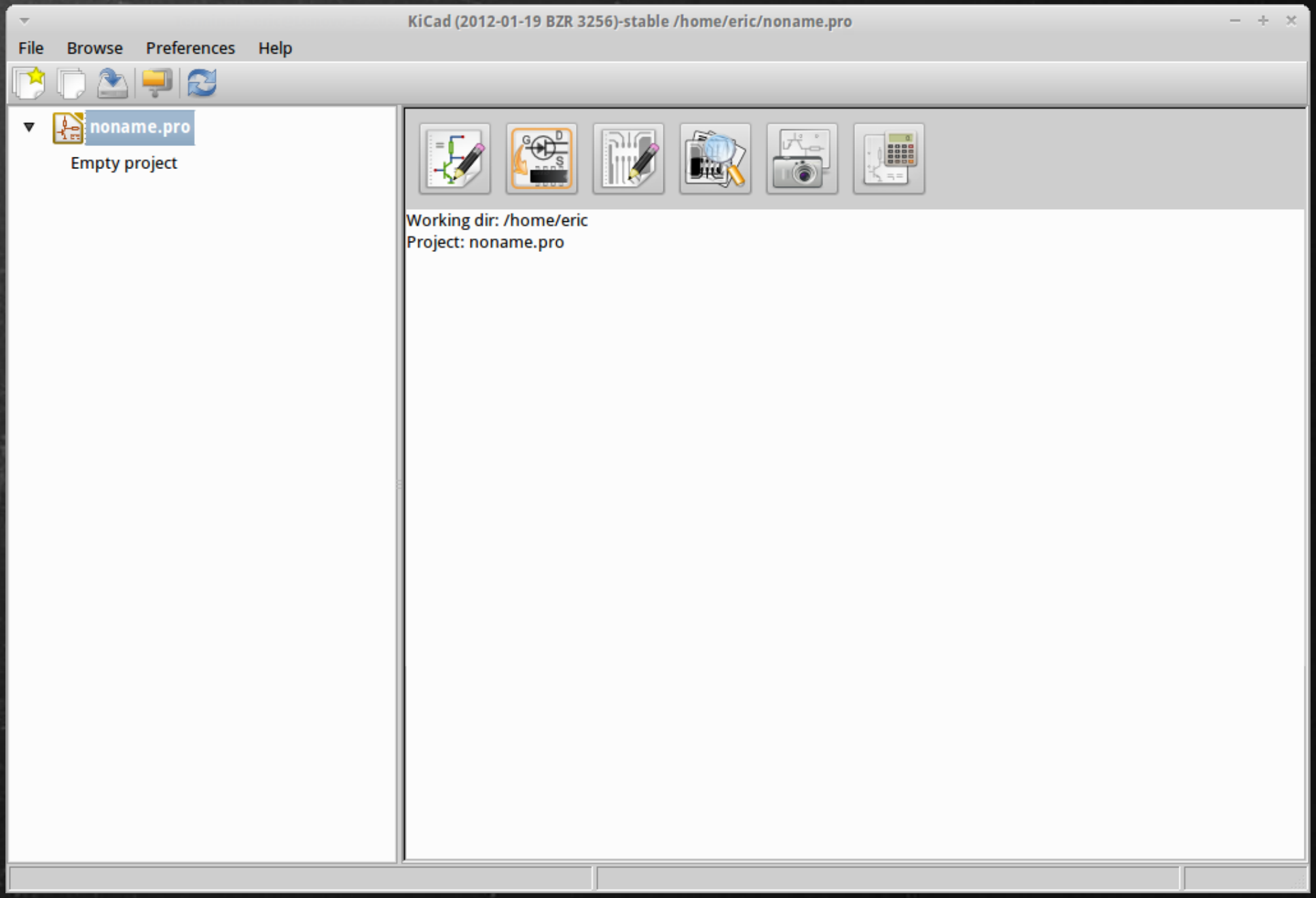
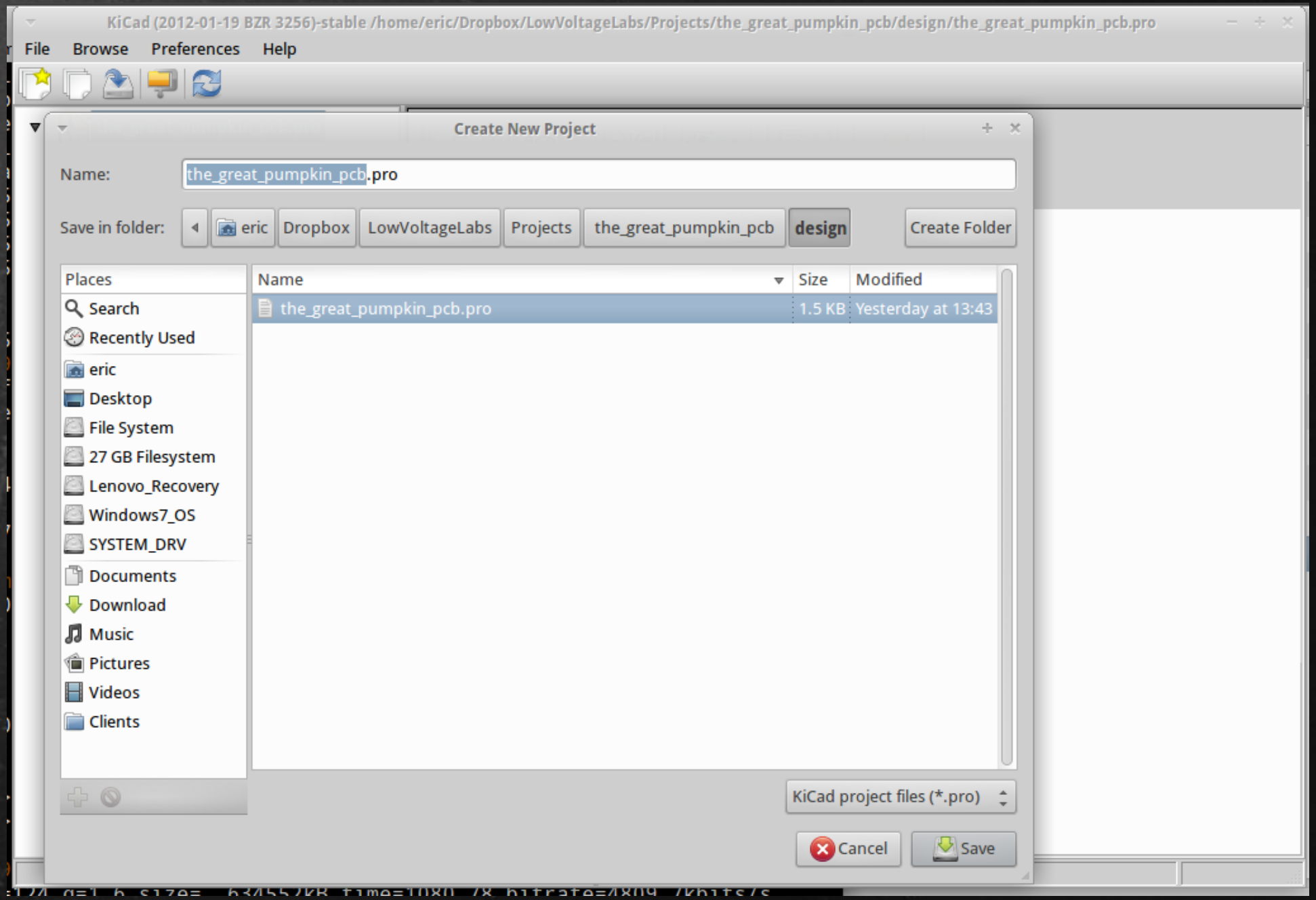

KiCad (2012-01-19 BZR 3256)-stable /home/eric/noname.pro
File
Browse
Preferences
Help
noname.pro
Empty project
Working dir: /home/eric
Project: noname.pro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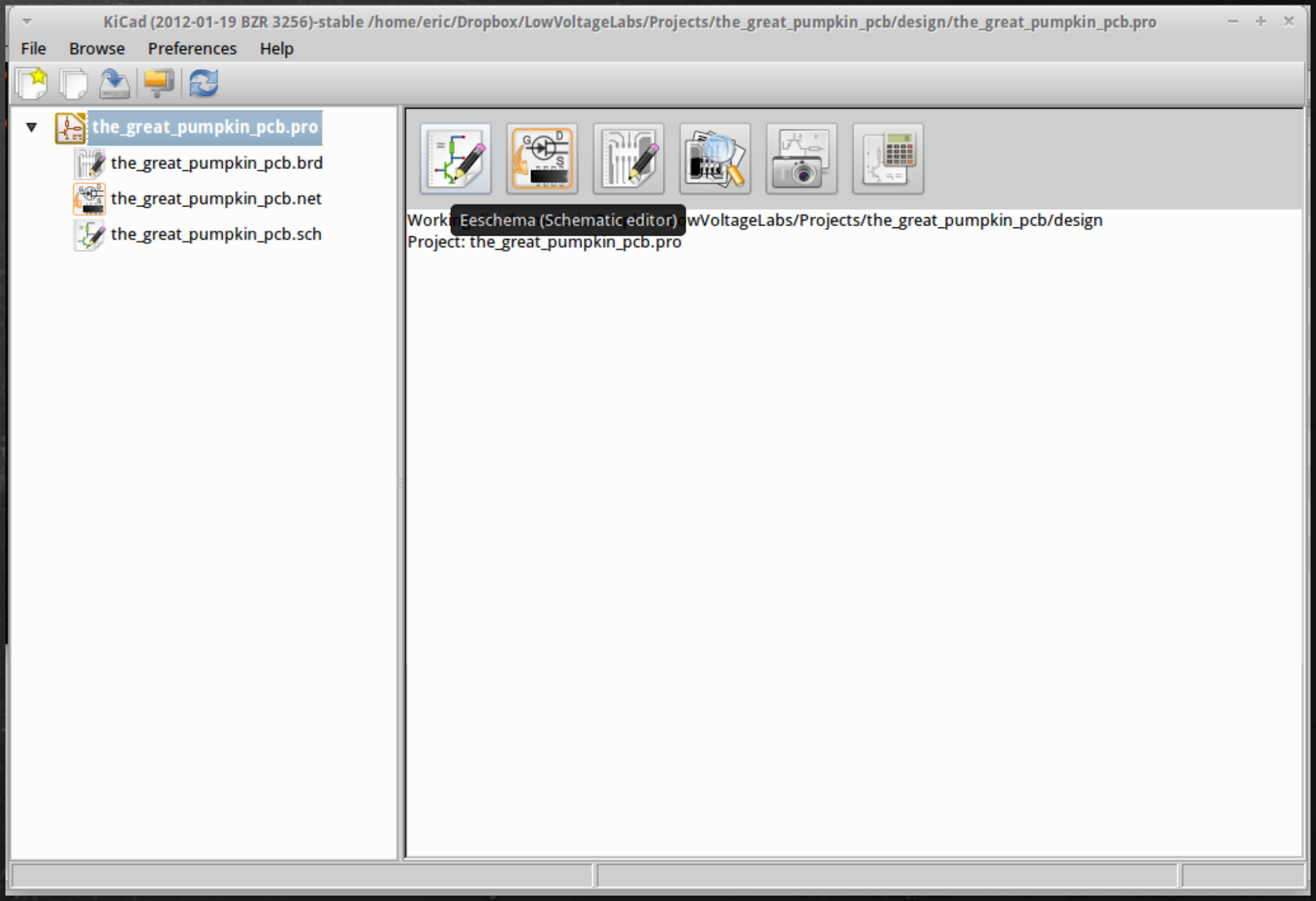
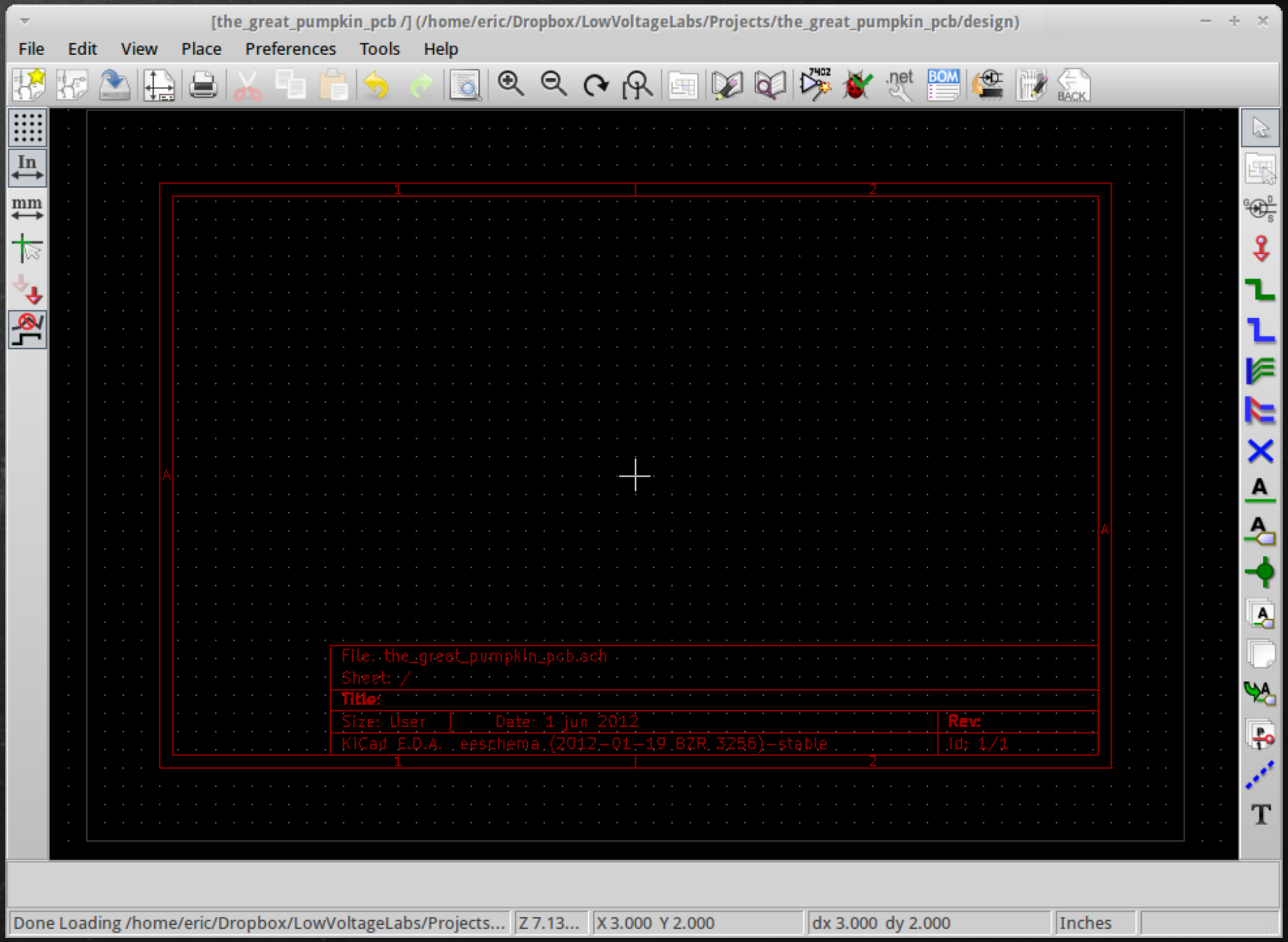
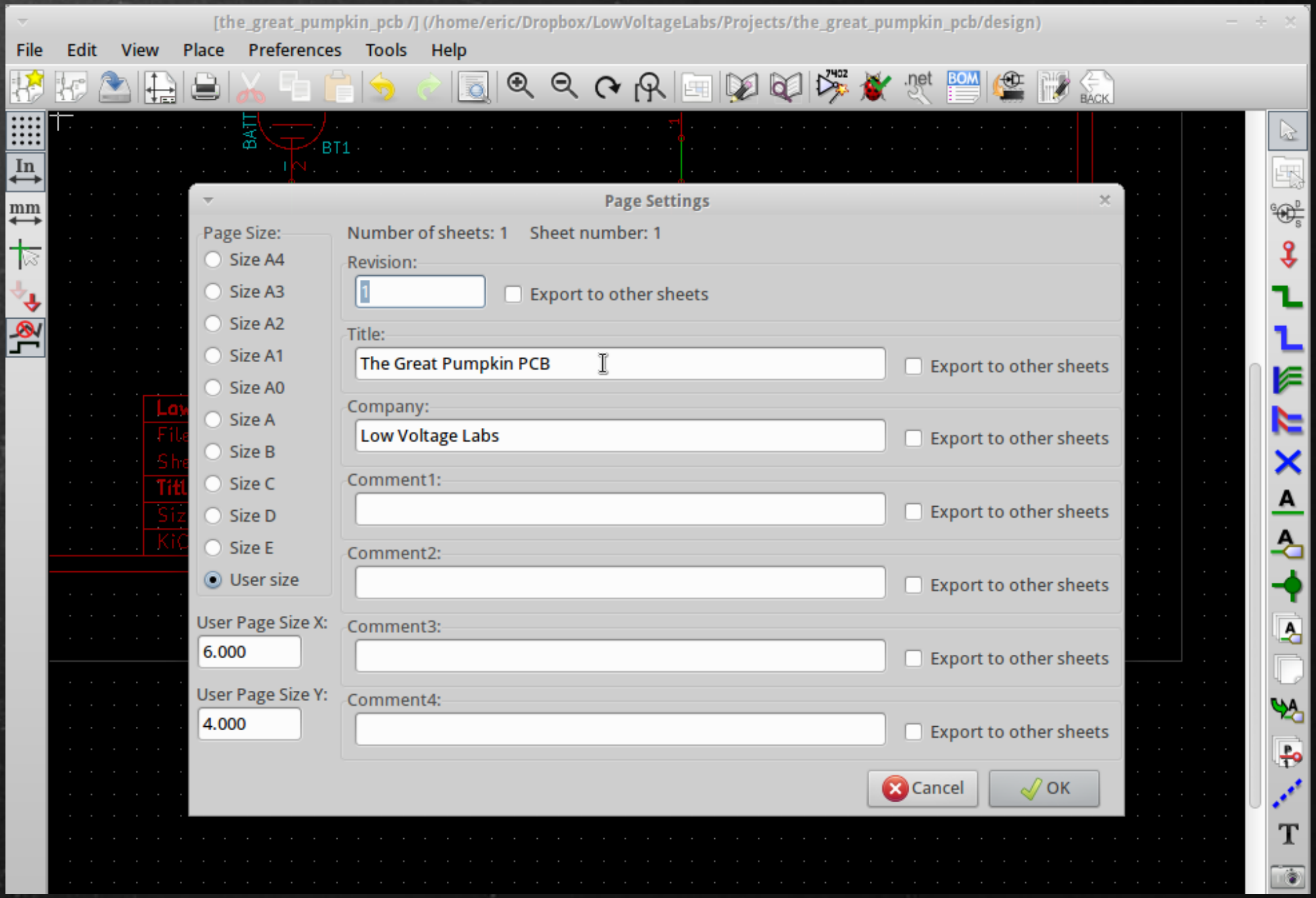
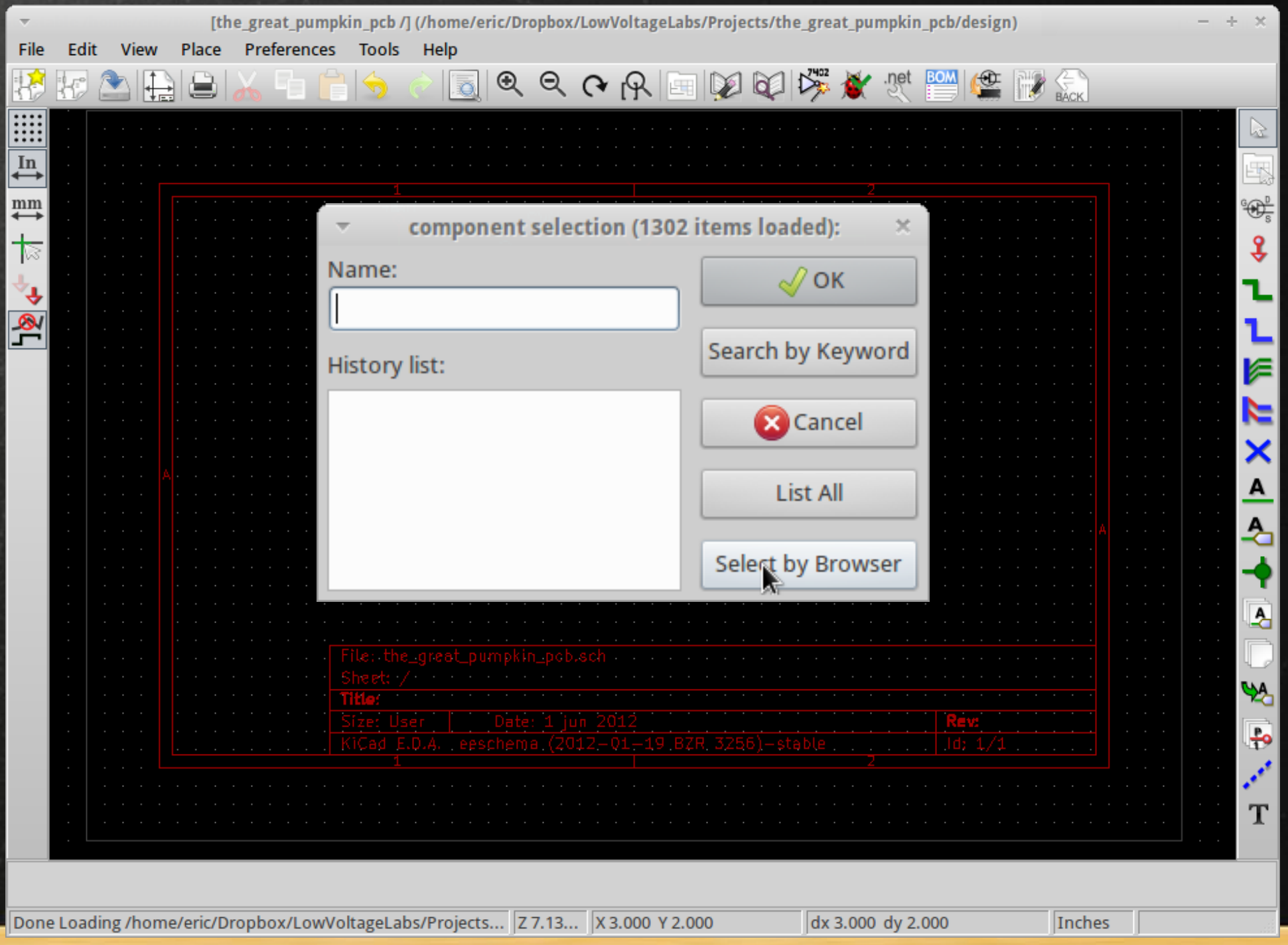
File
Browse
Preferences
Help
Create New Project
Name:
the_great_pumpkin_pcb.pro
Save in folder:
eric
Dropbox
LowVoltageLabs
Projects
the_great_pumpkin_pcb
design
Create Folder
Places
Search
Recently Used
eric
Desktop
File System
27 GB Filesystem
Lenovo_Recovery
Windows7_OS
SYSTEM_DRV
Documents
Download
Music
Pictures
Videos
Clients
Name
Size
Modified
the_great_pumpkin_pcb.pro
1.5 KB
Yesterday at 13:43
KiCad project files (*.pro)
Cancel
Save

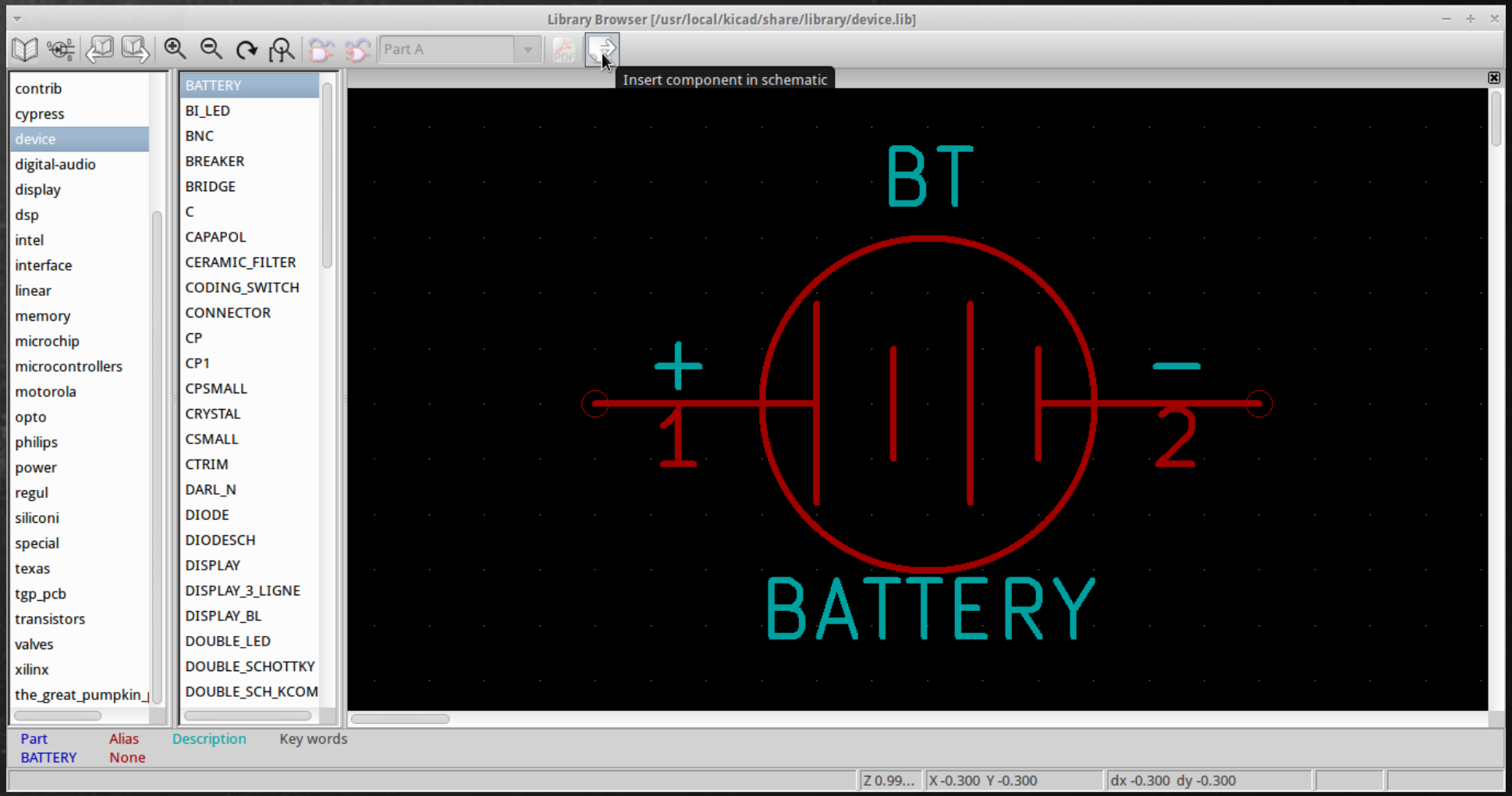

KiCad (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.pro
File
Browse
Preferences
Help
the_great_pumpkin_pcb.pro
the_great_pumpkin_pcb.brd
the_great_pumpkin_pcb.net
the_great_pumpkin_pcb.sch
Eeschema (Schematic editor)
wVoltageLabs/Projects/the_great_pumpkin_pcb/design
Project: the_great_pumpkin_pcb.pro

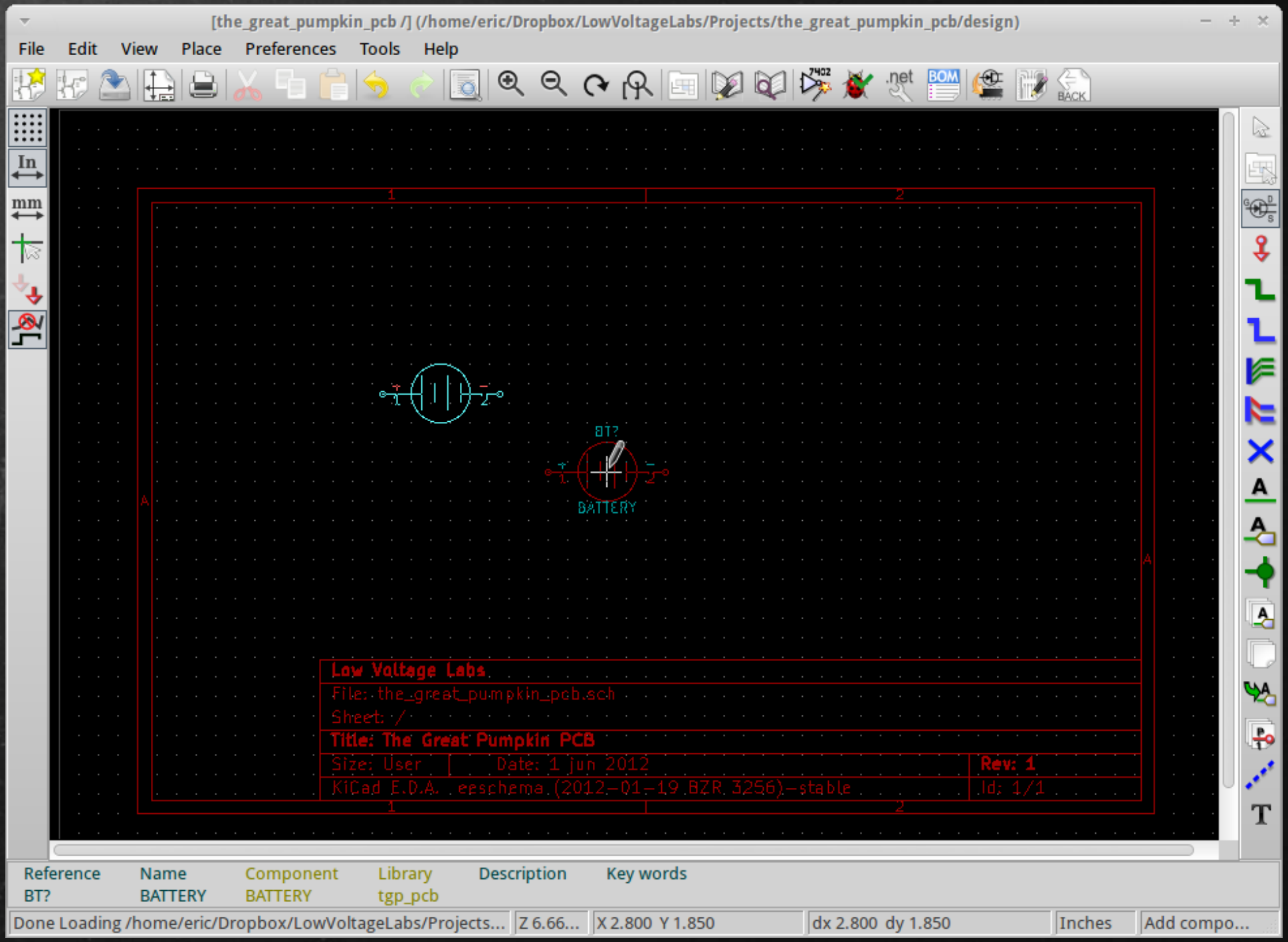

[the_great_pumpkin_pcb /] (/home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design)
File Edit View Place Preferences Tools Help
BACK
File: the_great_pumpkin_pcb.sch
Sheet: /
Title:
Size: User
Date: 1 jun 2012
Rev:
KiCad E.D.A. eeschema (2012-01-19 BZR 3256)-stable
Id: 1/1
Done Loading /home/eric/Dropbox/LowVoltageLabs/Projects...
Z 7.13...
X 3.000 Y 2.000
dx 3.000 dy 2.000
Inches


[the_great_pumpkin_pcb /] (/home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design)
File Edit View Place Preferences Tools Help
BATT
BT1
Page Settings
Page Size:
Size A4
Size A3
Size A2
Size A1
Size A0
Size A
Size B
Size C
Size D
Size E
User size
User Page Size X:
6.000
User Page Size Y:
4.000
Number of sheets: 1 Sheet number: 1
Revision:
1
Export to other sheets
Title:
The Great Pumpkin PCB
Export to other sheets
Company:
Low Voltage Labs
Export to other sheets
Comment1:
Export to other sheets
Comment2:
Export to other sheets
Comment3:
Export to other sheets
Comment4:
Export to other sheets
Cancel
OK

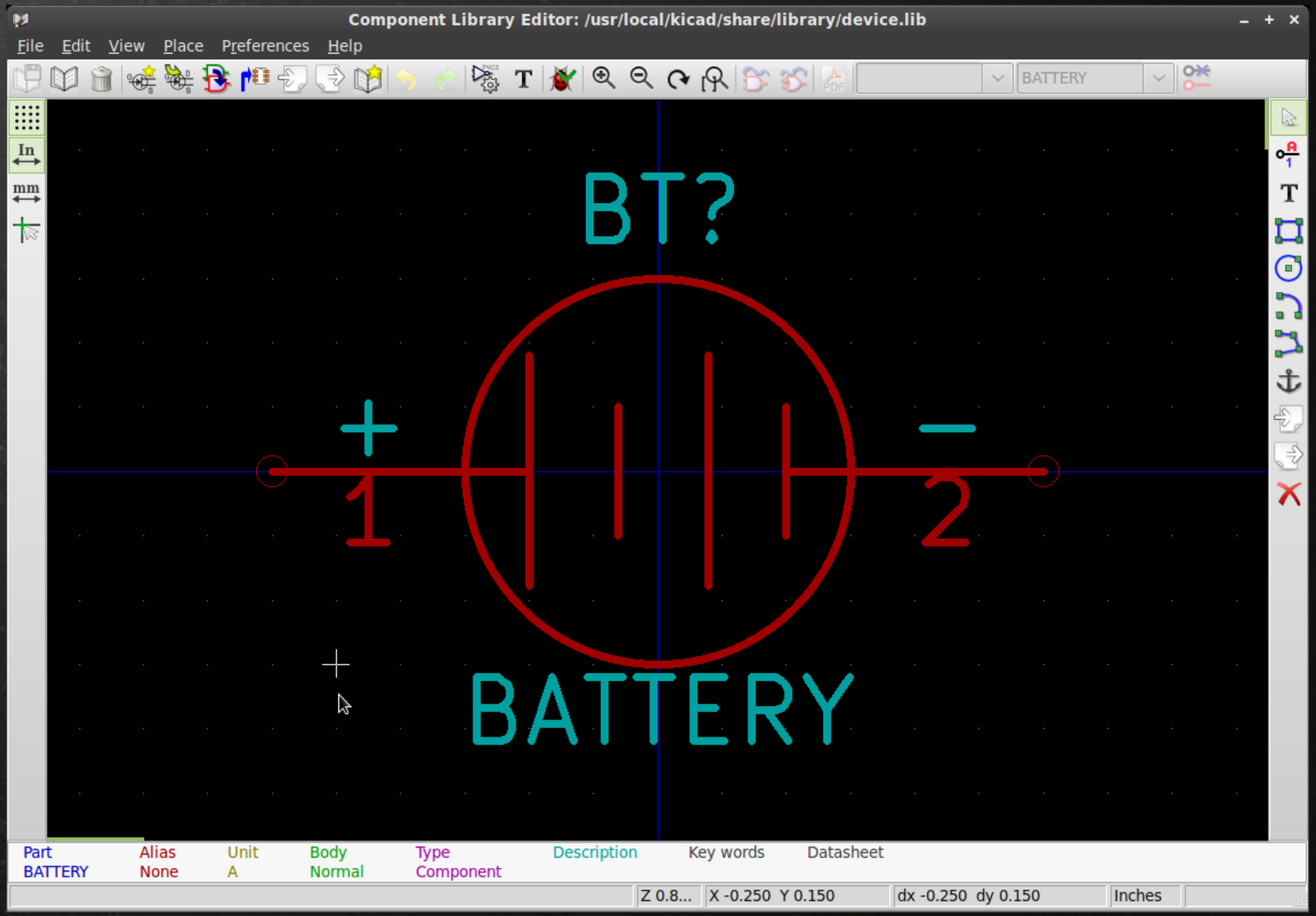
Add a component with shift-a

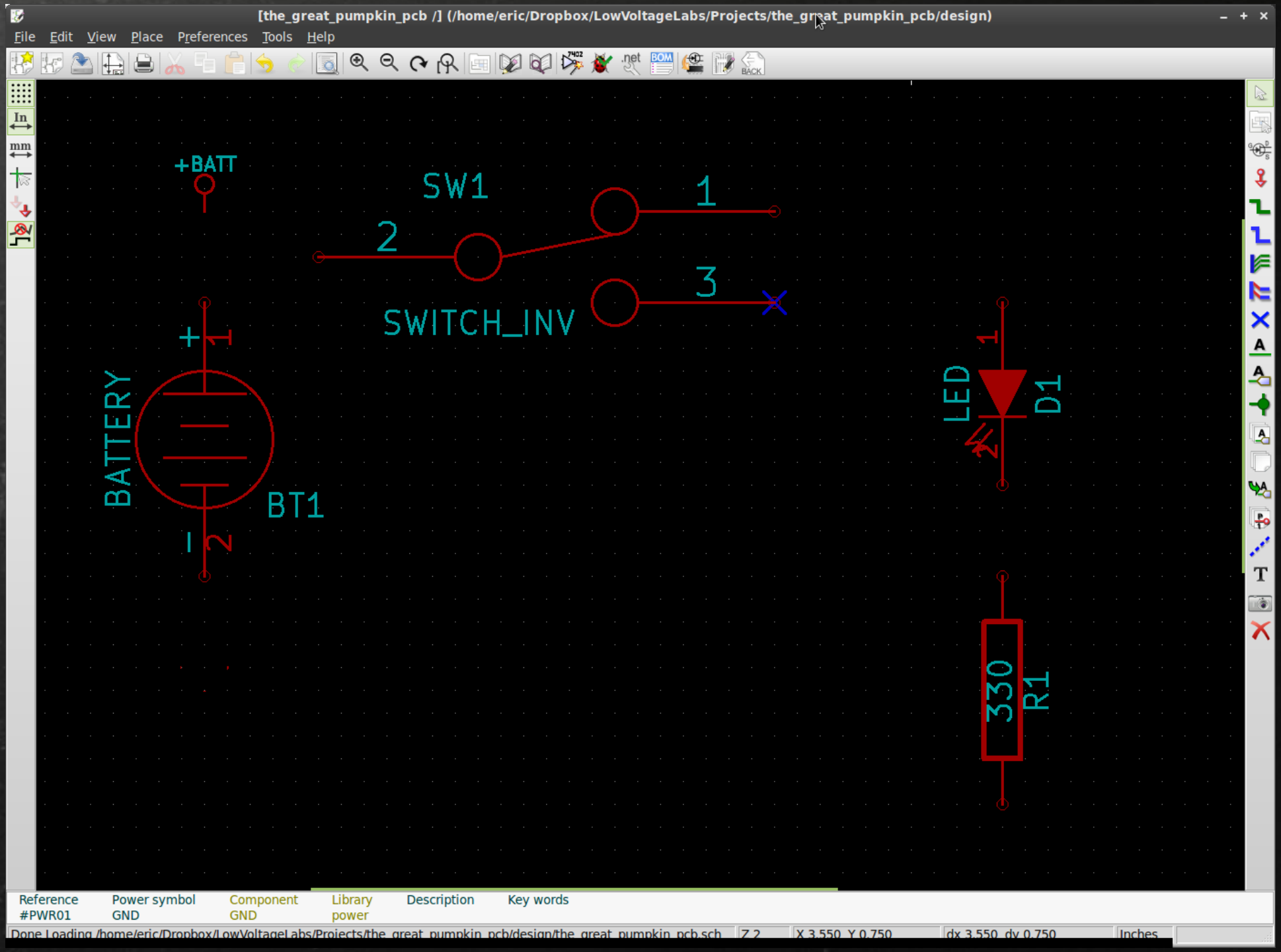



Library Browser [/usr/local/kicad/share/library/device.lib]
Part A
Insert component in schematic
contrib
cypress
device
digital-audio
display
dsp
intel
interface
linear
memory
microchip
microcontrollers
motorola
opto
philips
power
regul
siliconi
special
texas
tgp_pcb
transistors
valves
xilinx
the_great_pumpkin_
BATTERY
BI_LED
BNC
BREAKER
BRIDGE
C
CAPAPOL
CERAMIC_FILTER
CODING_SWITCH
CONNECTOR
CP
CP1
CPSMALL
CRYSTAL
CSMALL
CTRIM
DARL_N
DIODE
DIODESCH
DISPLAY
DISPLAY_3_LIGNE
DISPLAY_BL
DOUBLE_LED
DOUBLE_SCHOTTKY
DOUBLE_SCH_KCOM
BT
+
1
2
BATTERY
Part
BATTERY
Alias
None
Description
Key words
Z 0.99...
X -0.300 Y -0.300
dx -0.300 dy -0.300

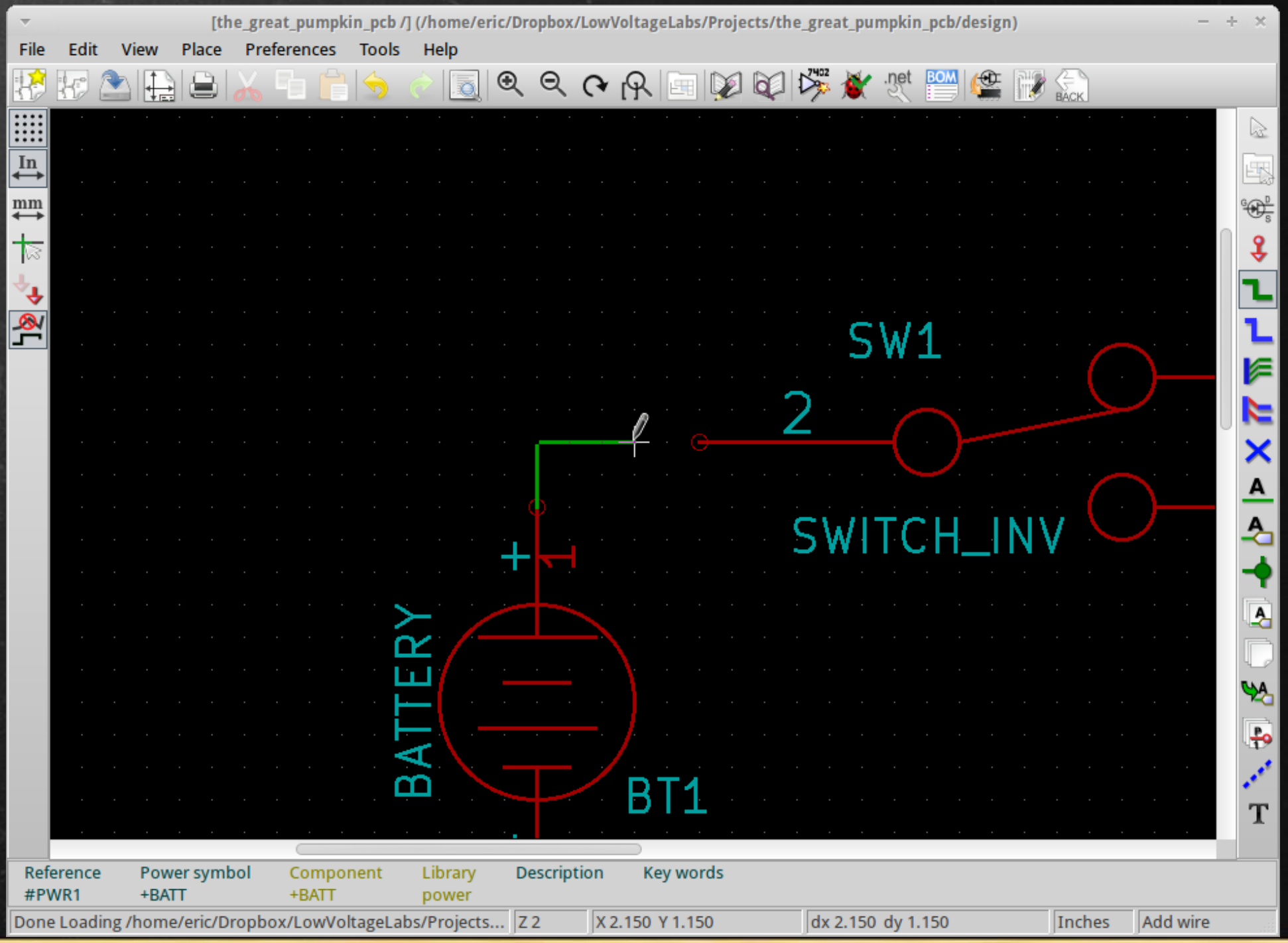

[the_great_pumpkin_pcb /] (/home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design)
File Edit View Place Preferences Tools Help
BT?
BATTERY
Low Voltage Labs
File: the_great_pumpkin_pcb.sch
Sheet: /
Title: The Great Pumpkin PCB
Size: User
Date: 1 jun 2012
Rev: 1
KiCad E.D.A. eeschema (2012-01-19 BZR 3256)-stable
Id: 1/1
Reference Name Component Library Description Key words
BT? BATTERY BATTERY tgp_pcb
Done Loading /home/eric/Dropbox/LowVoltageLabs/Projects...
Z 6.66...
X 2.800 Y 1.850
dx 2.800 dy 1.850
Inches
Add compo...

Component editor

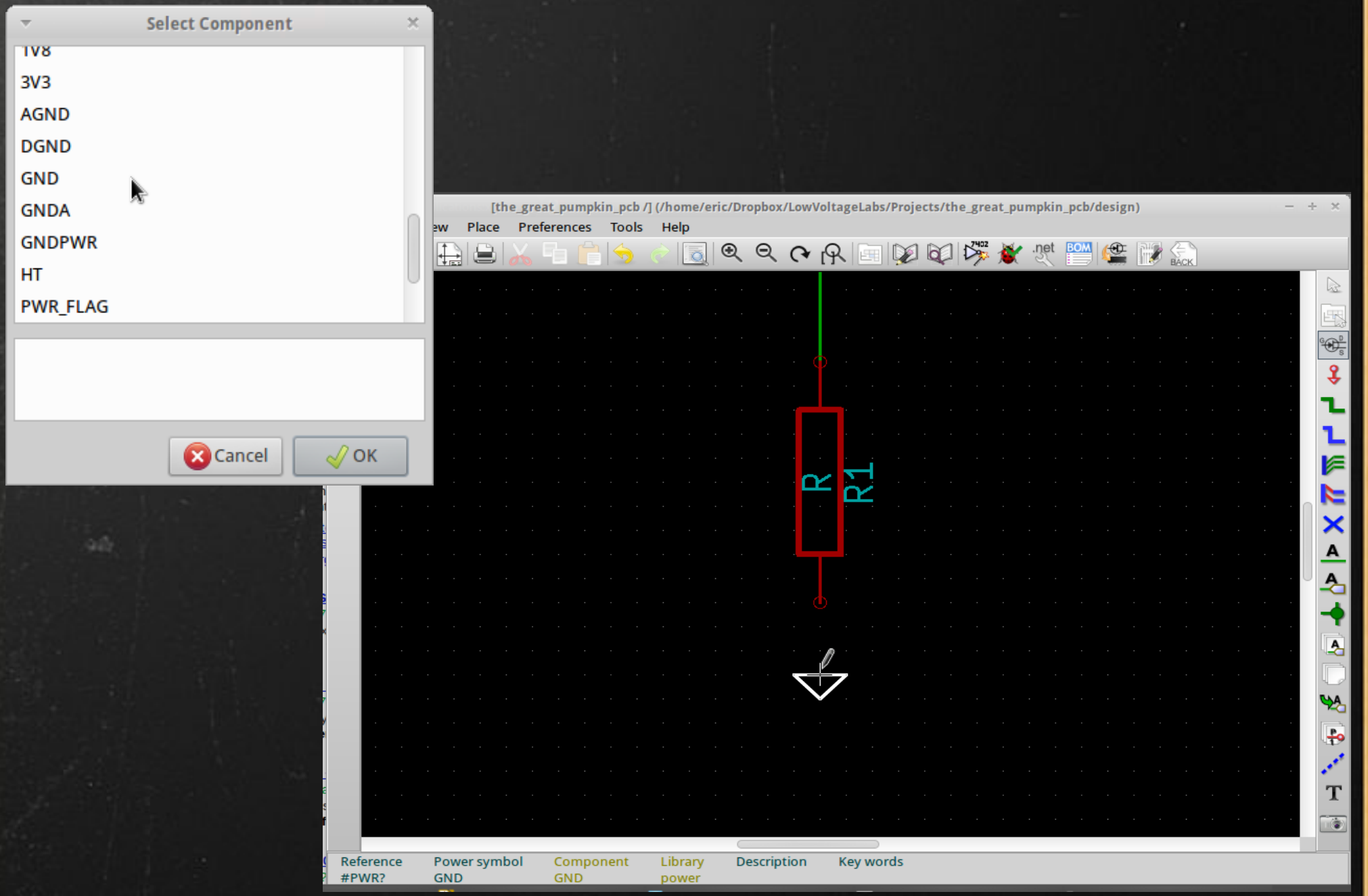


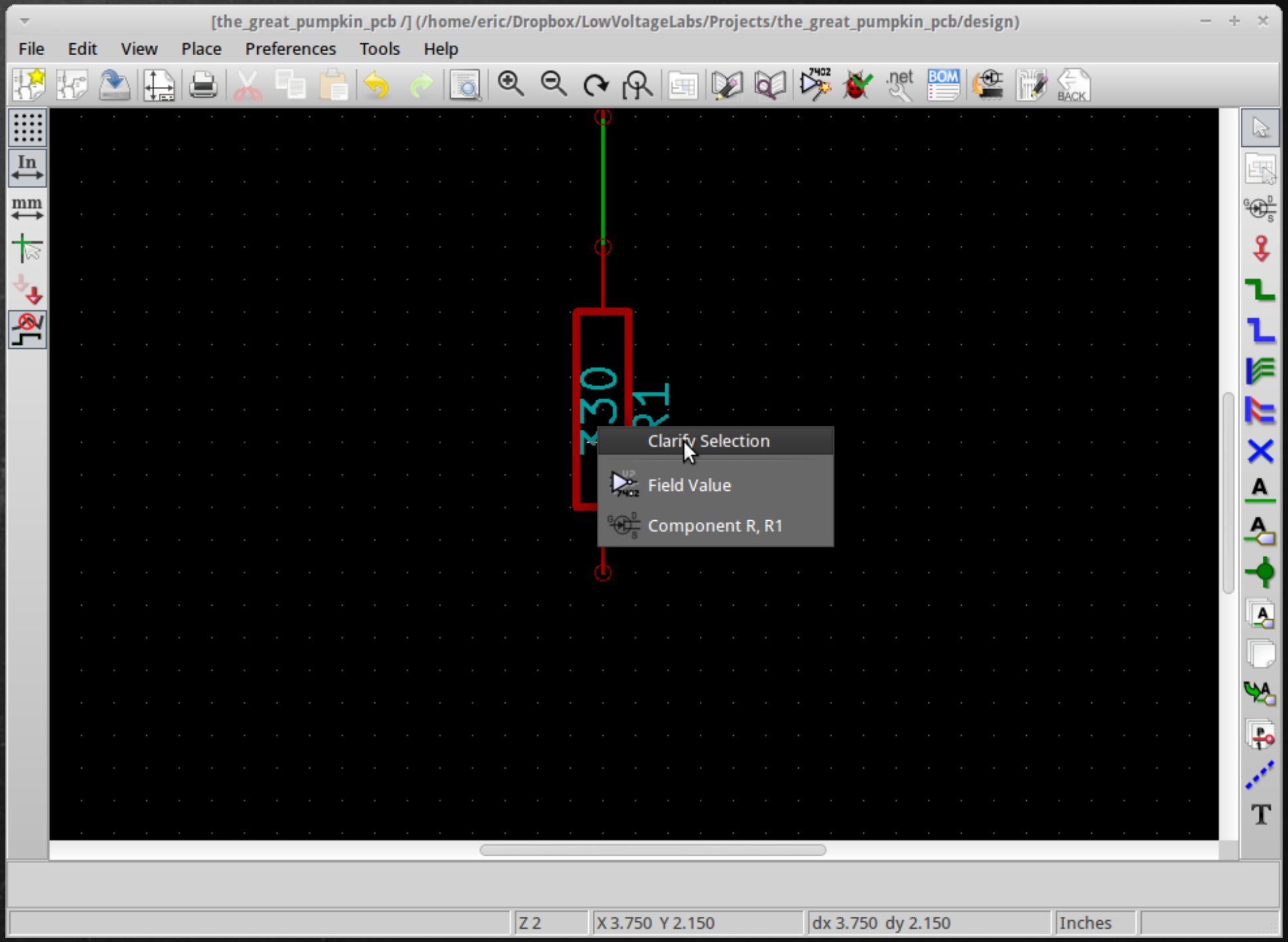

[the_great_pumpkin_pcb /] (/home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design)
File Edit View Place Preferences Tools Help
+BATT
SW1
1
2
3
SWITCH_INV
BATTERY
BT1
LED
D1
330
R1
Reference Power symbol Component Library Description Key words
#PWR01 GND GND power
Done Loading /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.sch
Z 2
X 3.550 Y 0.750
dx 3.550 dy 0.750
Inches

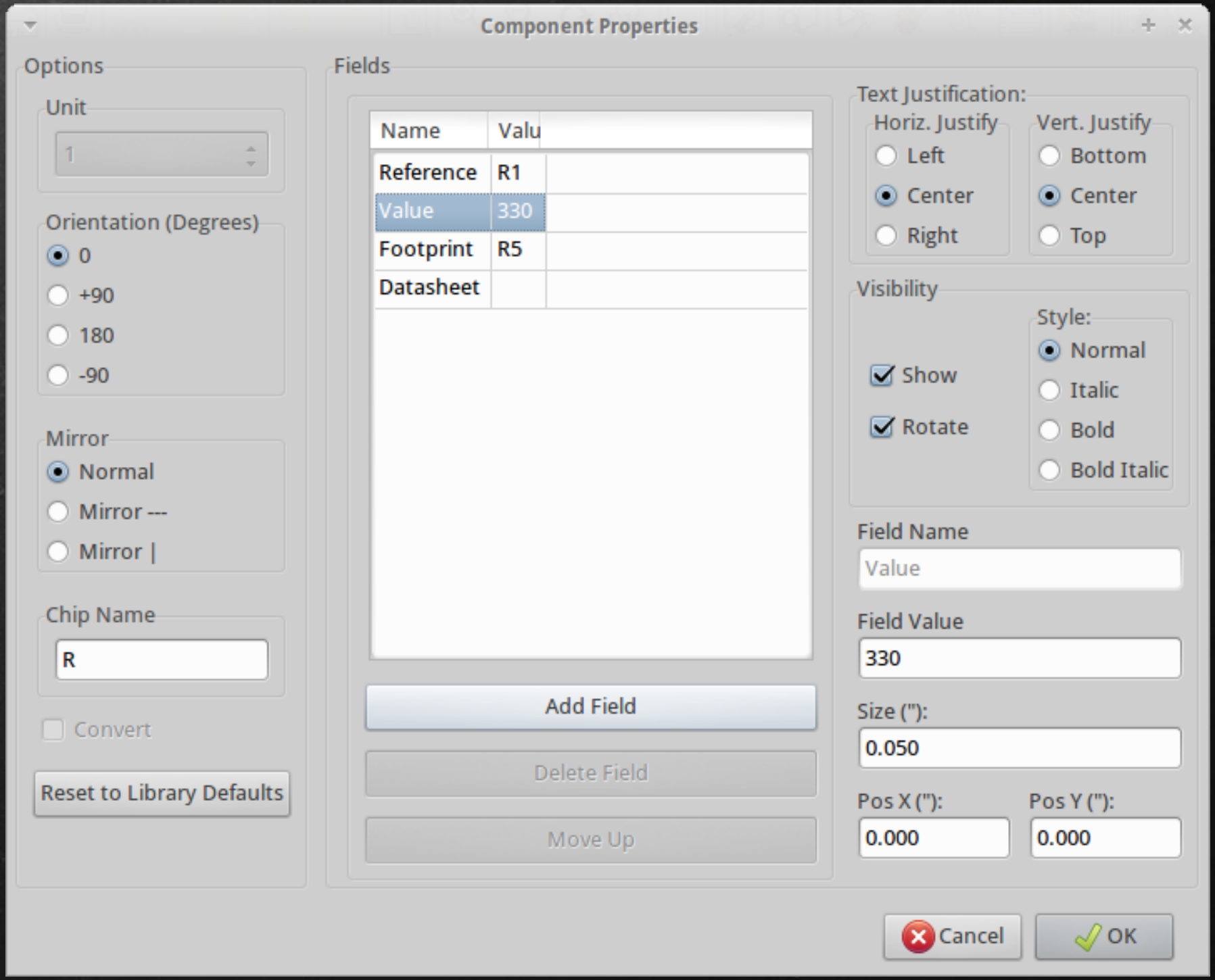
Add wires with shift-w



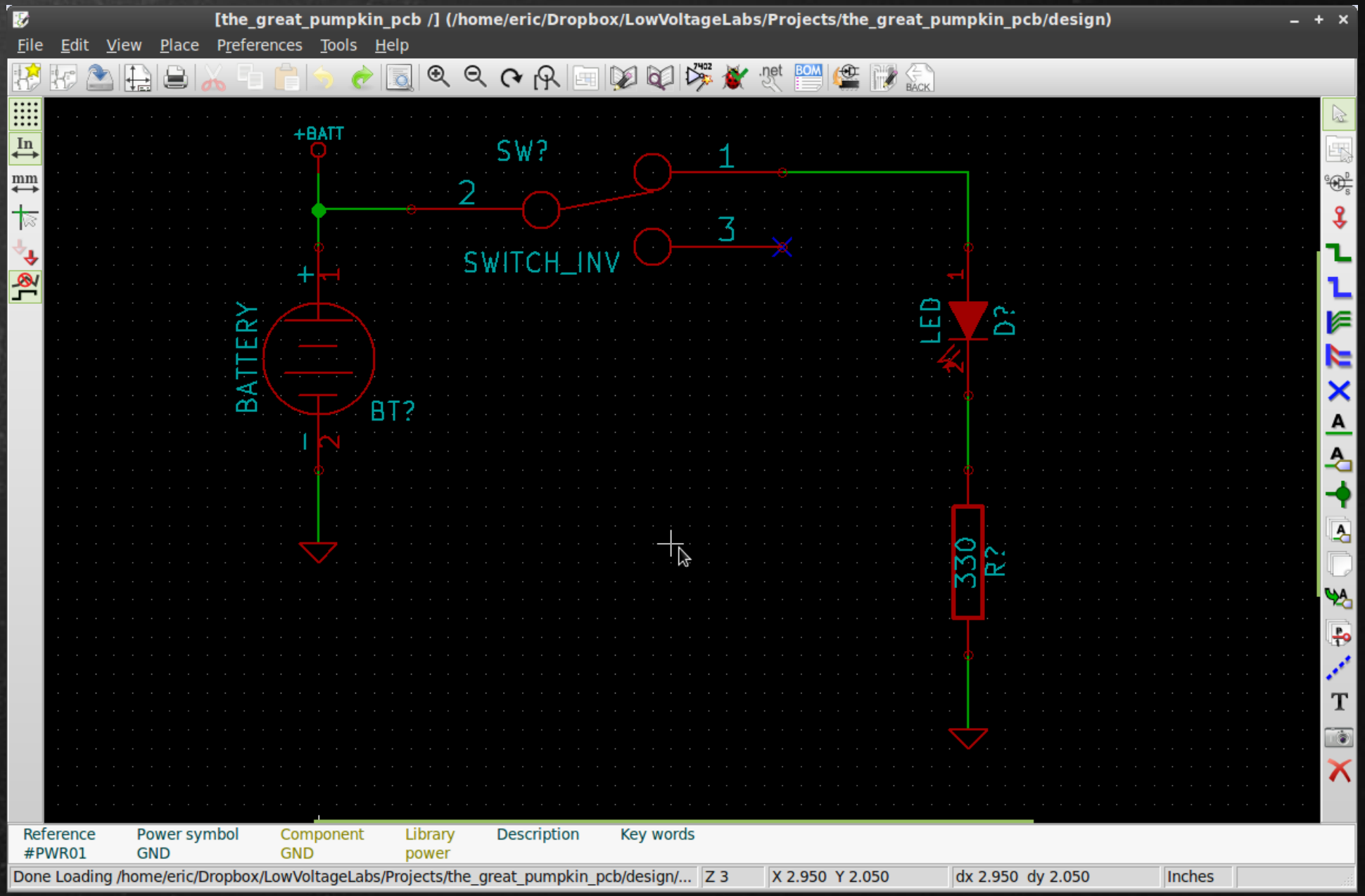
Placing power and GND symbols, shift-P



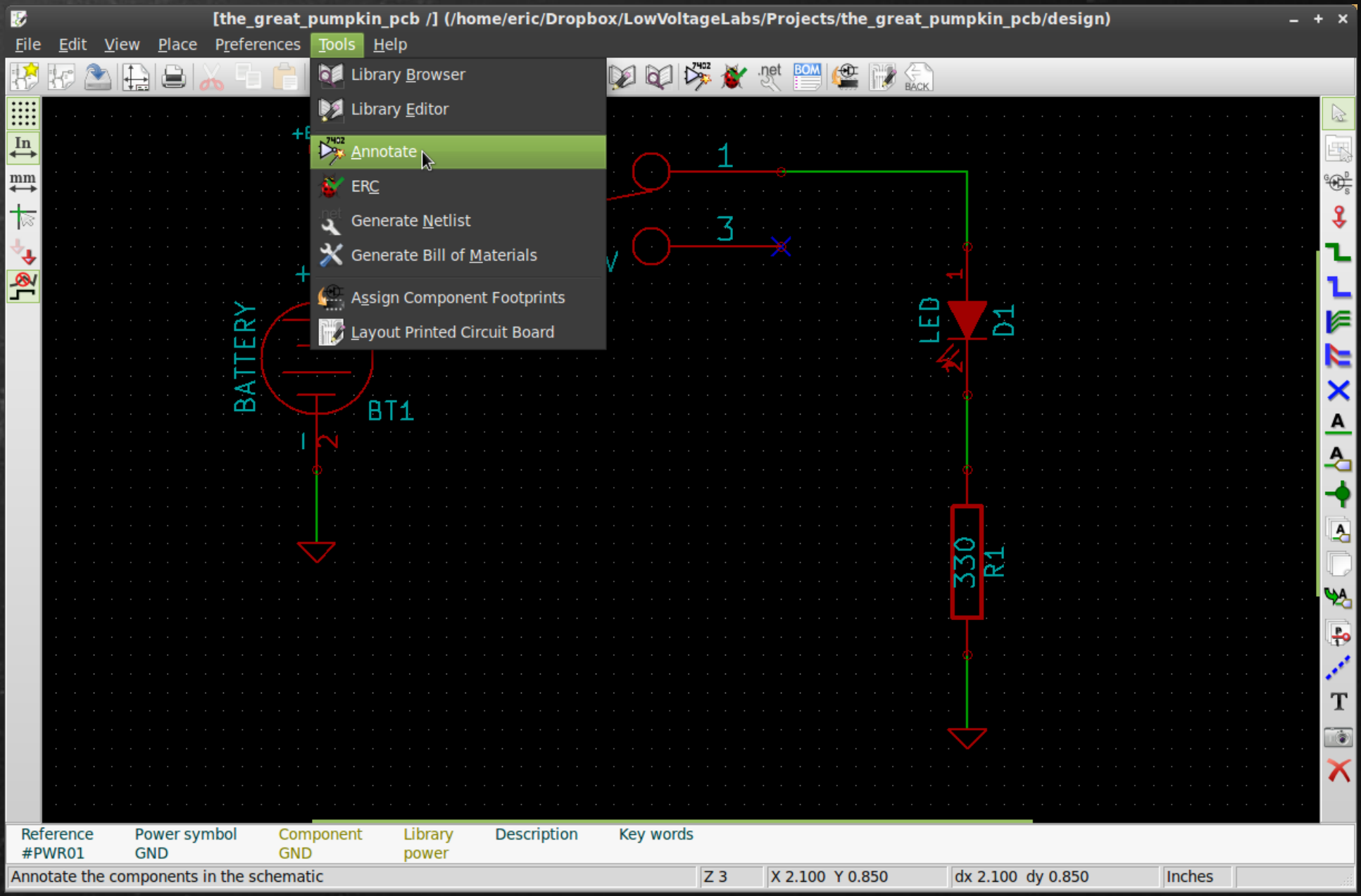

[the_great_pumpkin_pcb /] (/home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design)
File
Edit
View
Place
Preferences
Tools
Help
In
mm
BACK
Clarify Selection
Field Value
Component R, R1
Z 2
X 3.750 Y 2.150
dx 3.750 dy 2.150
Inches

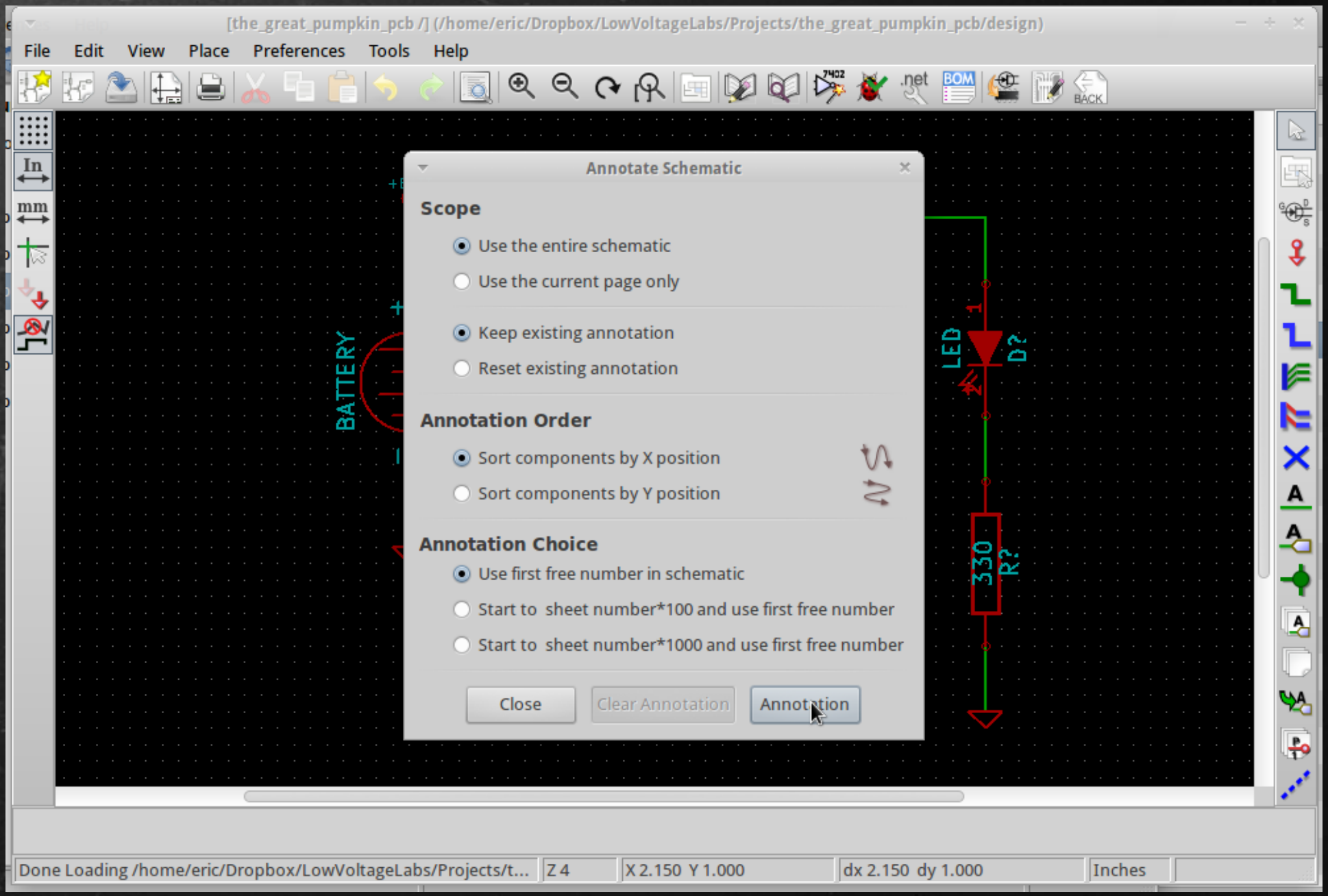

Component Properties
Options
Unit
1
Orientation (Degrees)
0
+90
180
-90
Mirror
Normal
Mirror ---
Mirror |
Chip Name
R
Convert
Reset to Library Defaults
Fields
Name
Valu
Reference
R1
Value
330
Footprint
R5
Datasheet
Add Field
Delete Field
Move Up
Text Justification:
Horiz. Justify
Left
Center
Right
Vert. Justify
Bottom
Center
Top
Visibility
Show
Rotate
Style:
Normal
Italic
Bold
Bold Italic
Field Name
Value
Field Value
330
Size ("):
0.050
Pos X ("):
0.000
Pos Y ("):
0.000
Cancel
OK

Almost finished with the schematic

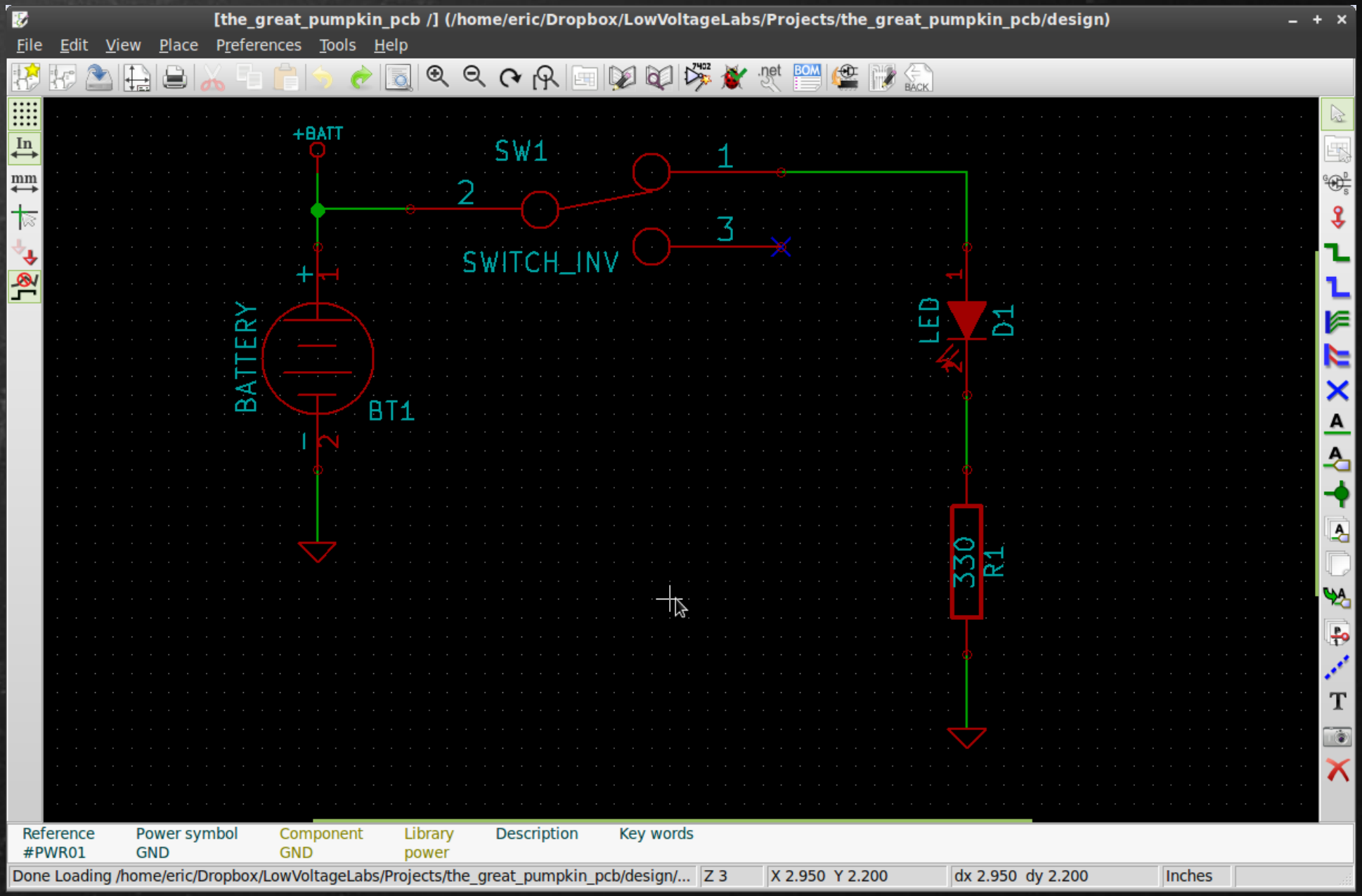


Annotate the schematic




[the_great_pumpkin_pcb /] (/home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design)
File
Edit
View
Place
Preferences
Tools
Help
Annotate Schematic
Scope
Use the entire schematic
Use the current page only
Keep existing annotation
Reset existing annotation
Annotation Order
Sort components by X position
Sort components by Y position
Annotation Choice
Use first free number in schematic
Start to sheet number*100 and use first free number
Start to sheet number*1000 and use first free number
Close
Clear Annotation
Annotation
BATTERY
LED
D?
330
R?
Done Loading /home/eric/Dropbox/LowVoltageLabs/Projects/t...
Z 4
X 2.150 Y 1.000
dx 2.150 dy 1.000
Inches

Finished schematic



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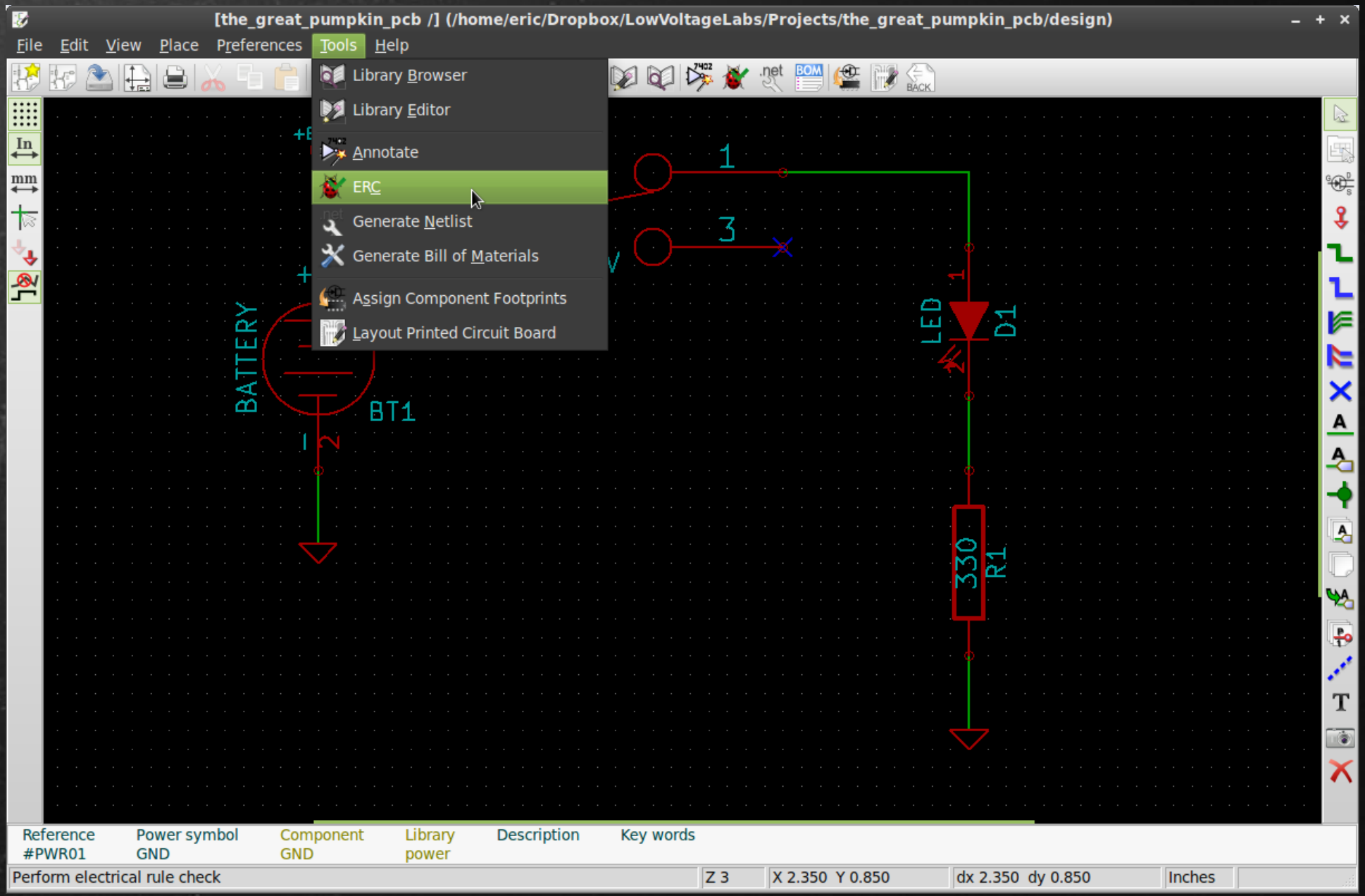
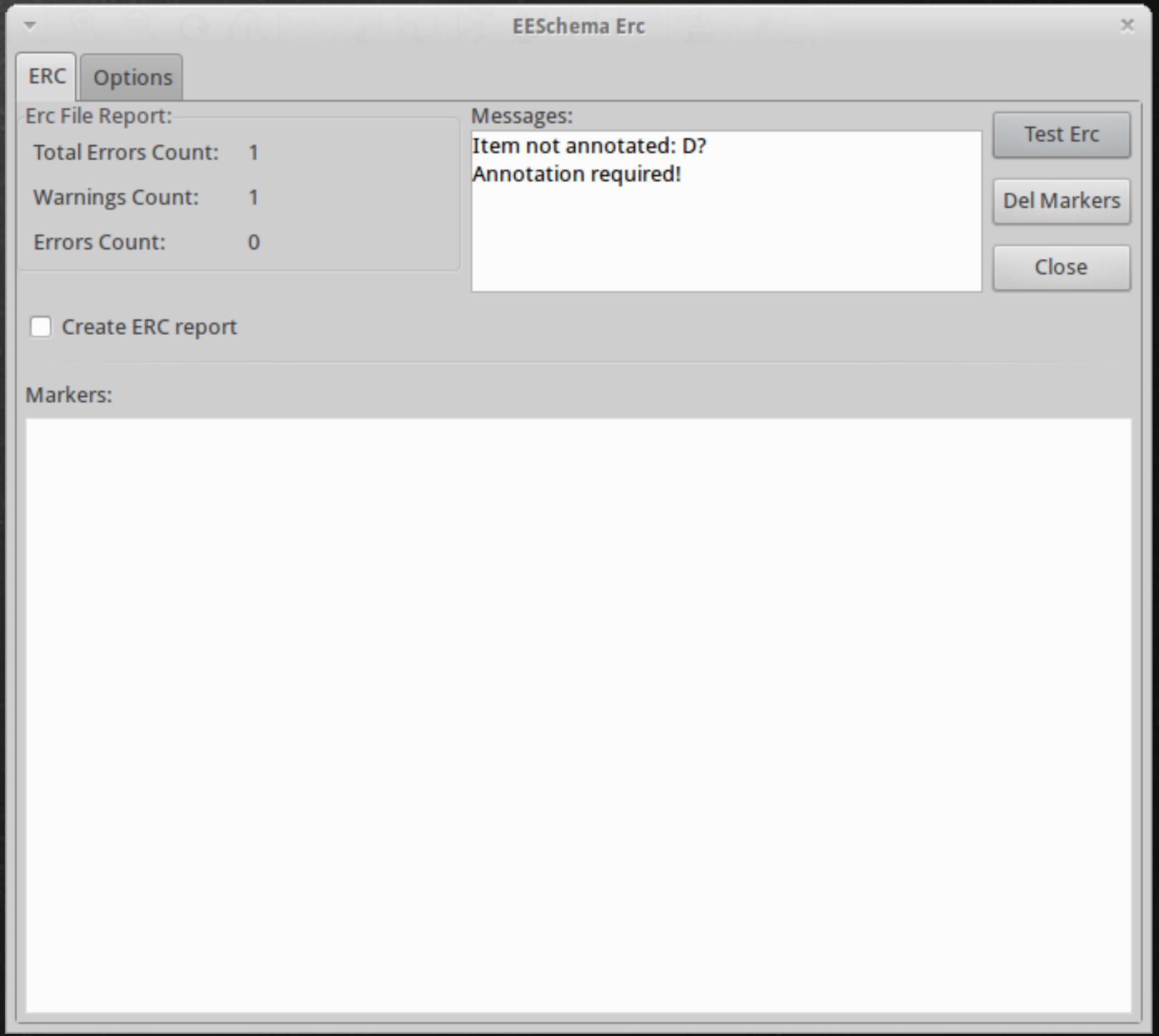
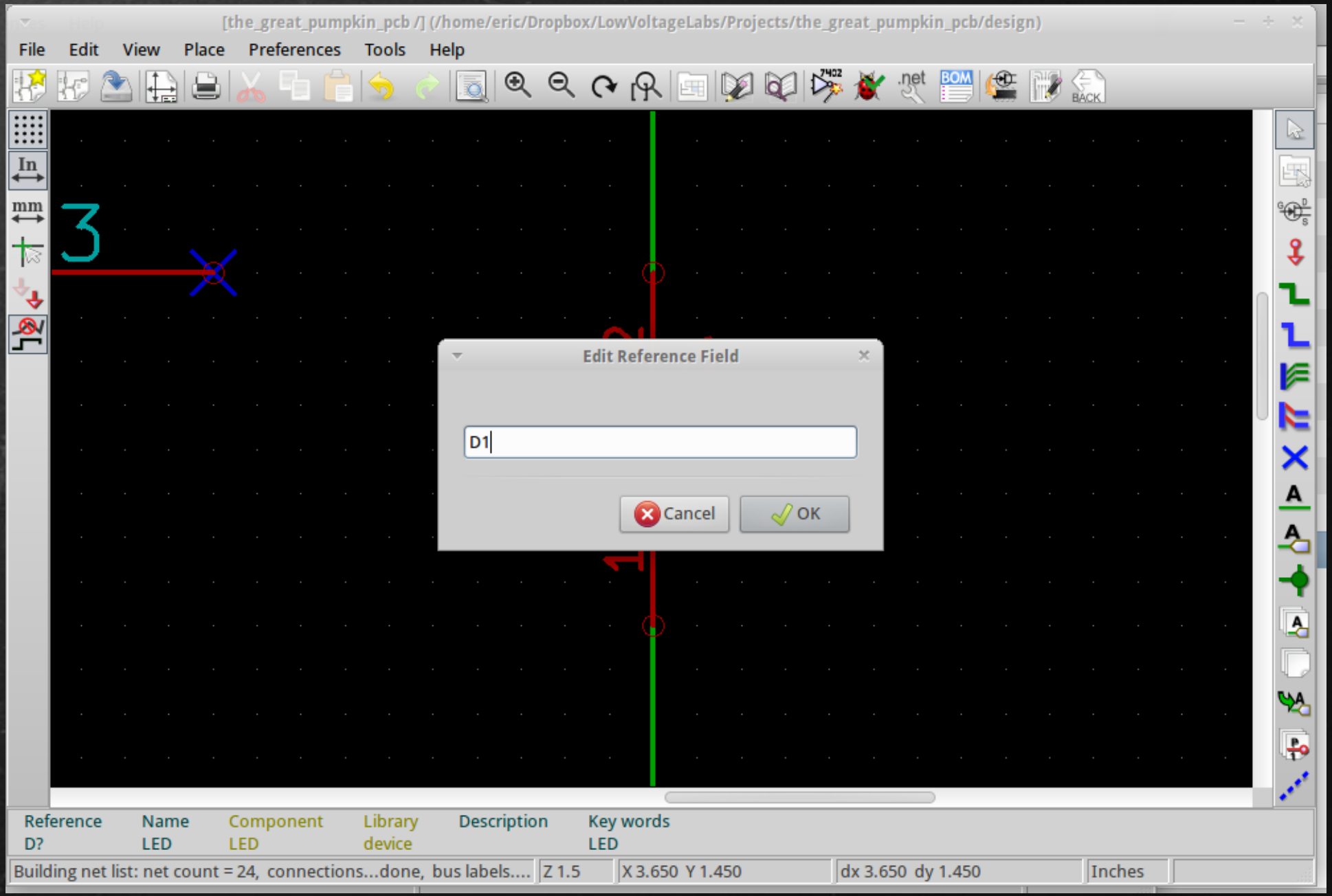
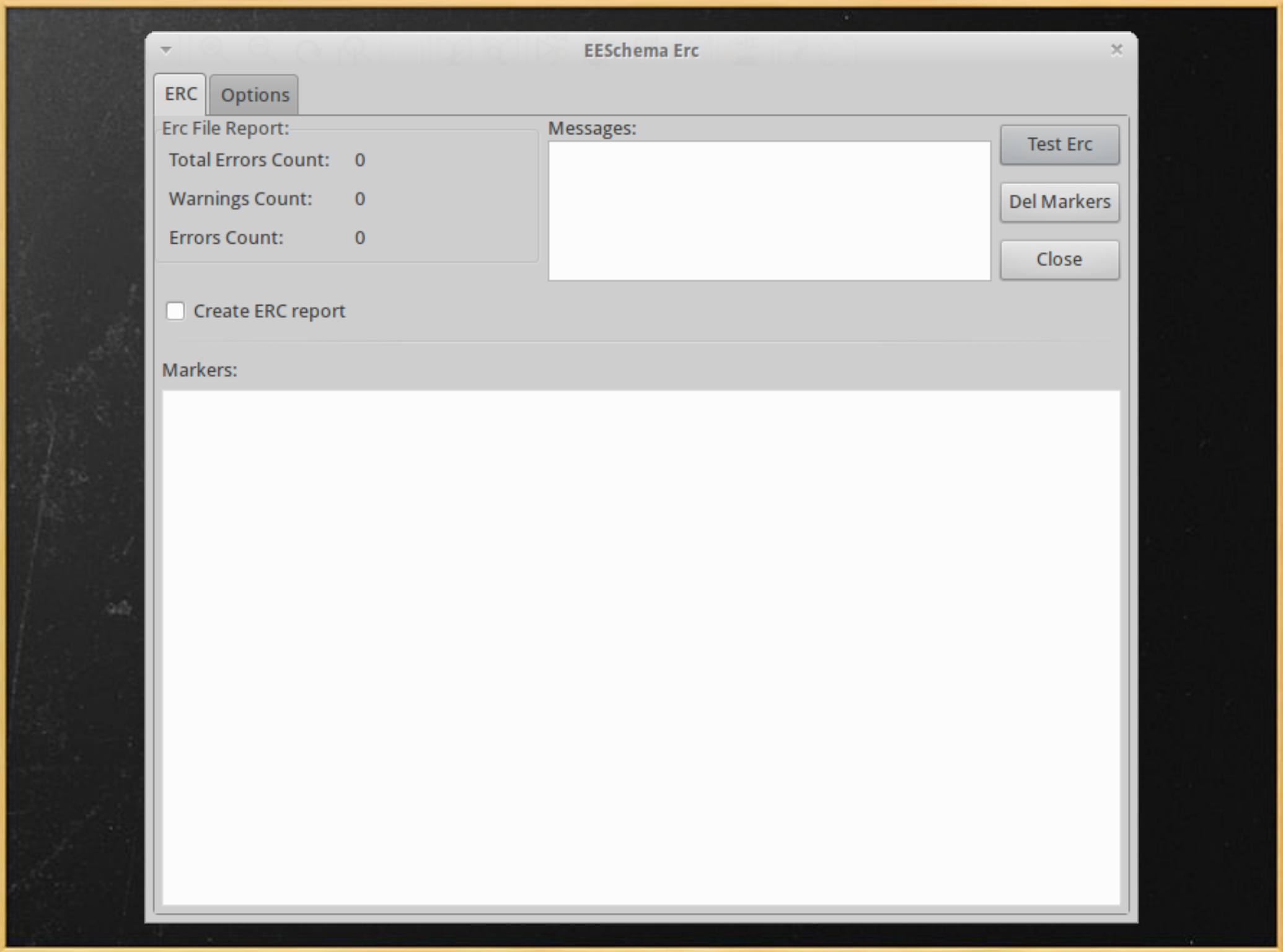
Error rule check the schematic

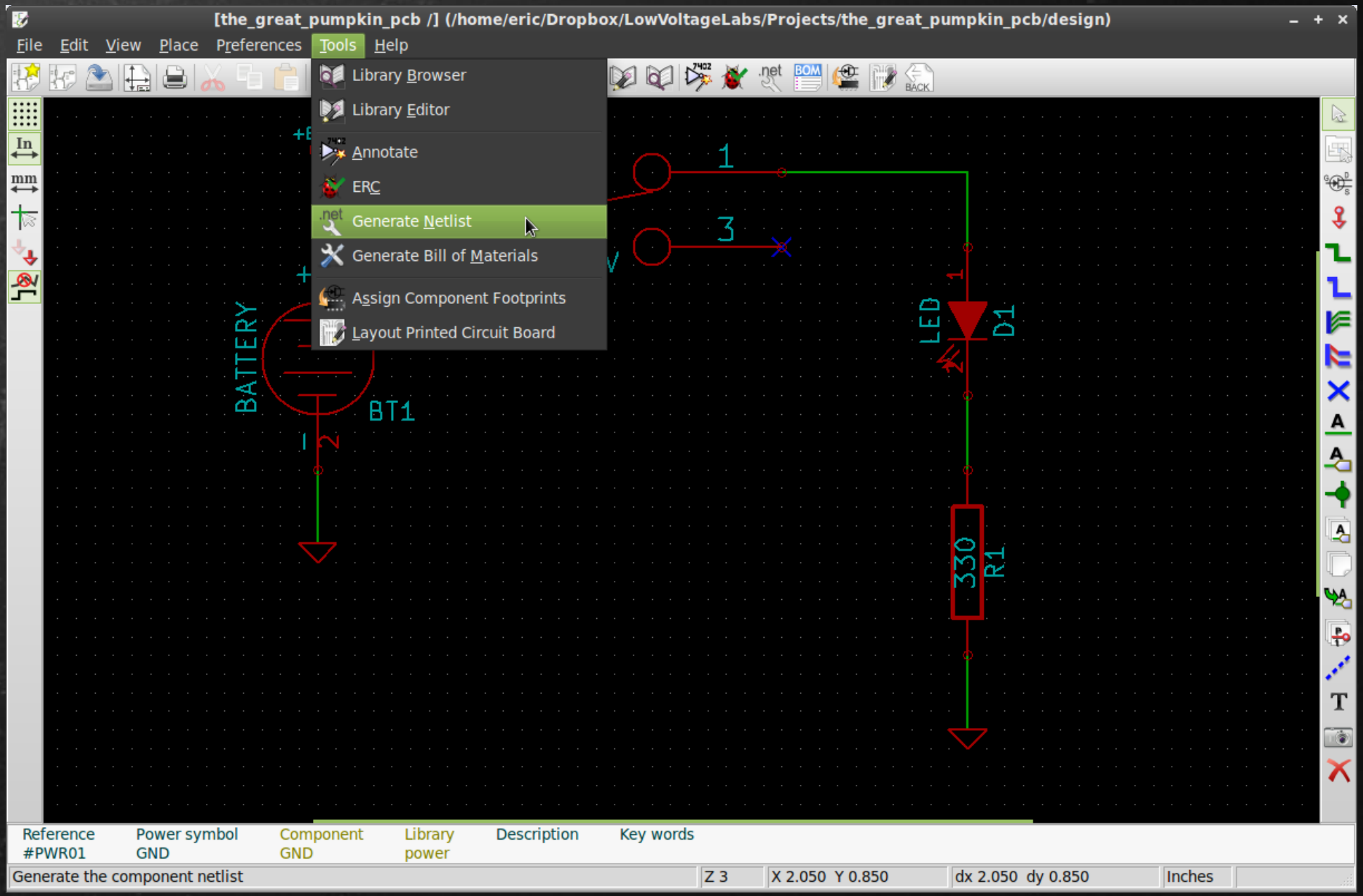


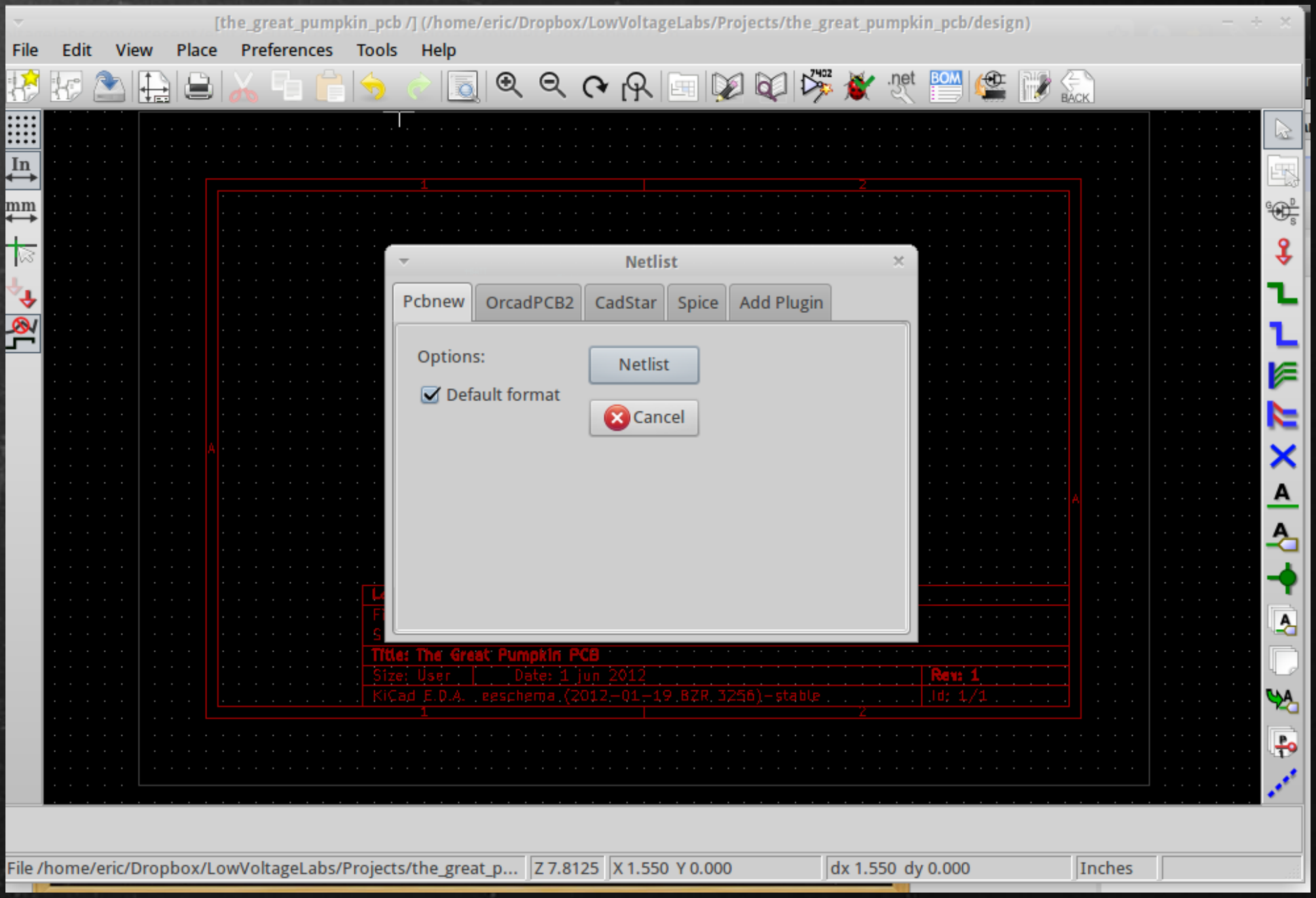

EESchema Erc
ERC
Options
Erc File Report:
Total Errors Count: 1
Warnings Count: 1
Errors Count: 0
Messages:
Item not annotated: D?
Annotation required!
Test Erc
Del Markers
Close
Create ERC report
Markers:


[the_great_pumpkin_pcb /] (/home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design)
File
Edit
View
Place
Preferences
Tools
Help
Edit Reference Field
D1
Cancel
OK
Reference
D?
Name
LED
Component
LED
Library
device
Description
Key words
LED
Building net list: net count = 24, connections...done, bus labels....
Z 1.5
X 3.650 Y 1.450
dx 3.650 dy 1.450
Inches


EESchema Erc
ERC
Options
Erc File Report:
Total Errors Count: 0
Warnings Count: 0
Errors Count: 0
Messages:
Test Erc
Del Markers
Close
Create ERC report
Markers:

Generate a netlist




[the_great_pumpkin_pcb /] (/home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design)
File
Edit
View
Place
Preferences
Tools
Help
Netlist
Pcbnew
OrcadPCB2
CadStar
Spice
Add Plugin
Options:
Default format
Netlist
Cancel
Title: The Great Pumpkin PCB
Size: User
Date: 1 jun 2012
Rev: 1
KiCad E.D.A. eeschema (2012-01-19 BZR 3256)-stable
Id: 1/1
File /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_p...
Z 7.8125
X 1.550 Y 0.000
dx 1.550 dy 0.000
Inches

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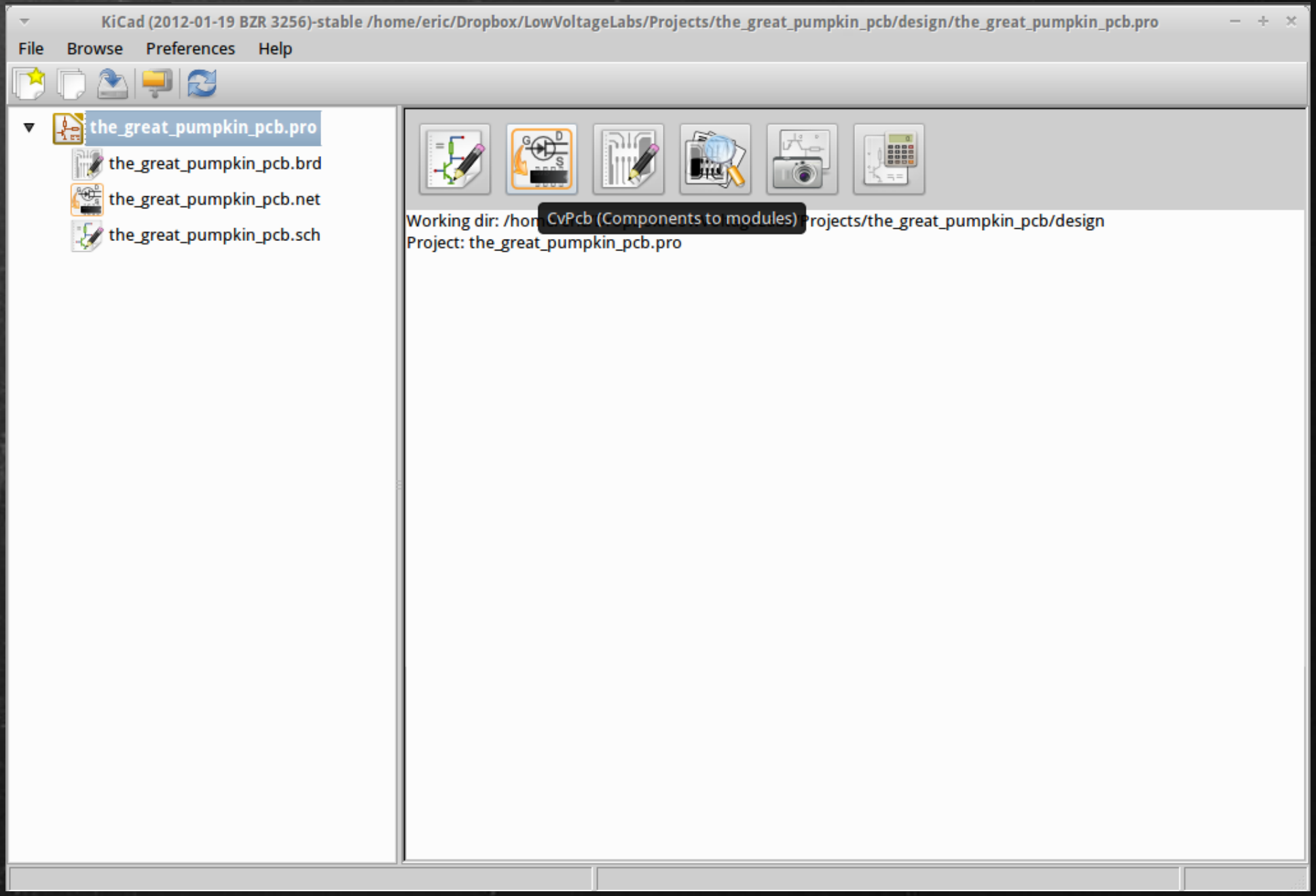
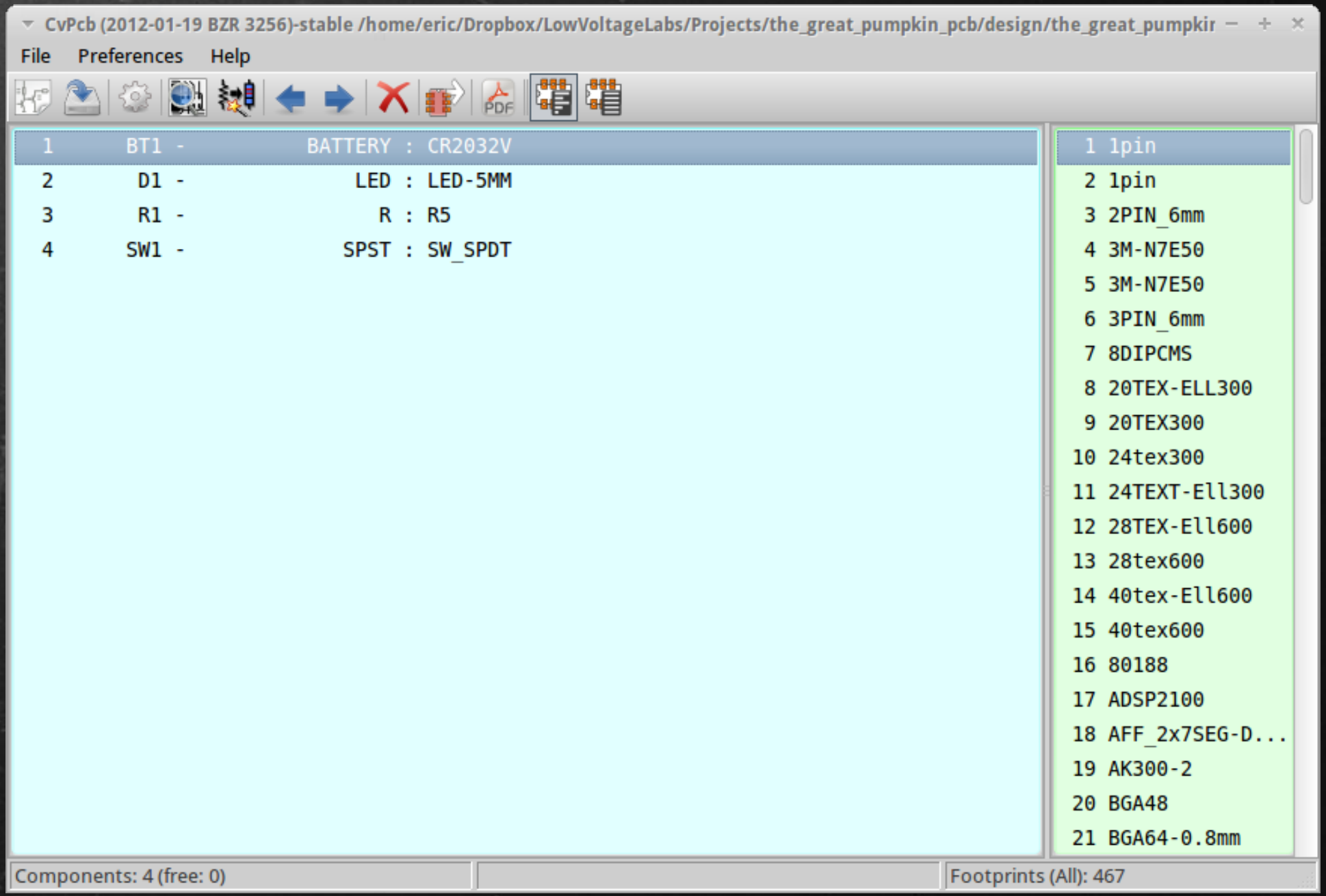
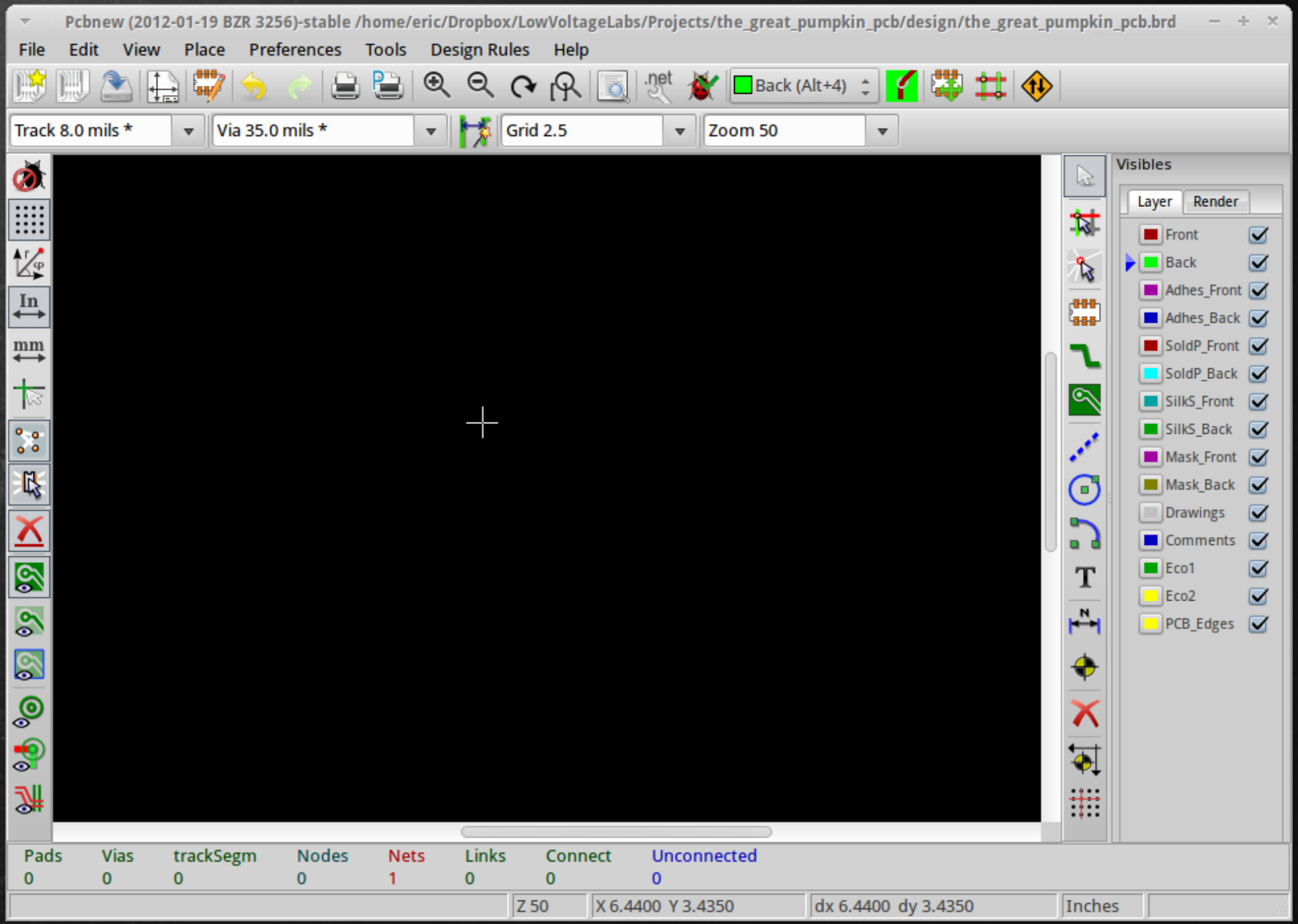

KiCad (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.pro
File
Browse
Preferences
Help
the_great_pumpkin_pcb.pro
the_great_pumpkin_pcb.brd
the_great_pumpkin_pcb.net
the_great_pumpkin_pcb.sch
CvPcb (Components to modules)
Working dir: /hom Projects/the_great_pumpkin_pcb/design
Project: the_great_pumpkin_pcb.pro

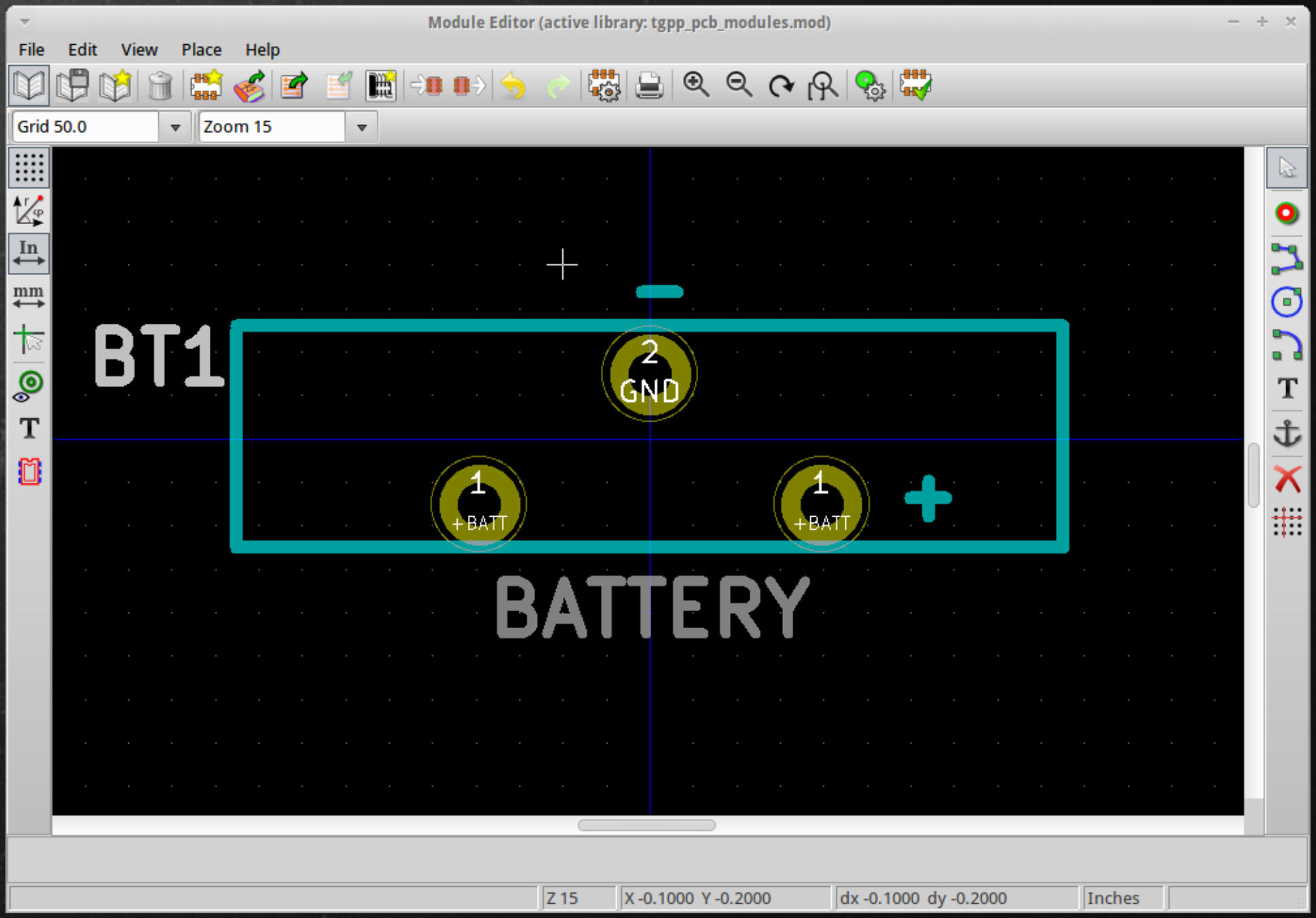

CvPcb (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkir
File
Preferences
Help
PDF
1 BT1 - BATTERY : CR2032V
2 D1 - LED : LED-5MM
3 R1 - R : R5
4 SW1 - SPST : SW_SPDT
1 1pin
2 1pin
3 2PIN_6mm
4 3M-N7E50
5 3M-N7E50
6 3PIN_6mm
7 8DIPCMS
8 20TEX-ELL300
9 20TEX300
10 24tex300
11 24TEXT-Ell300
12 28TEX-Ell600
13 28tex600
14 40tex-Ell600
15 40tex600
16 80188
17 ADSP2100
18 AFF_2x7SEG-D...
19 AK300-2
20 BGA48
21 BGA64-0.8mm
Components: 4 (free: 0)
Footprints (All): 467

Create a board with KiCAD

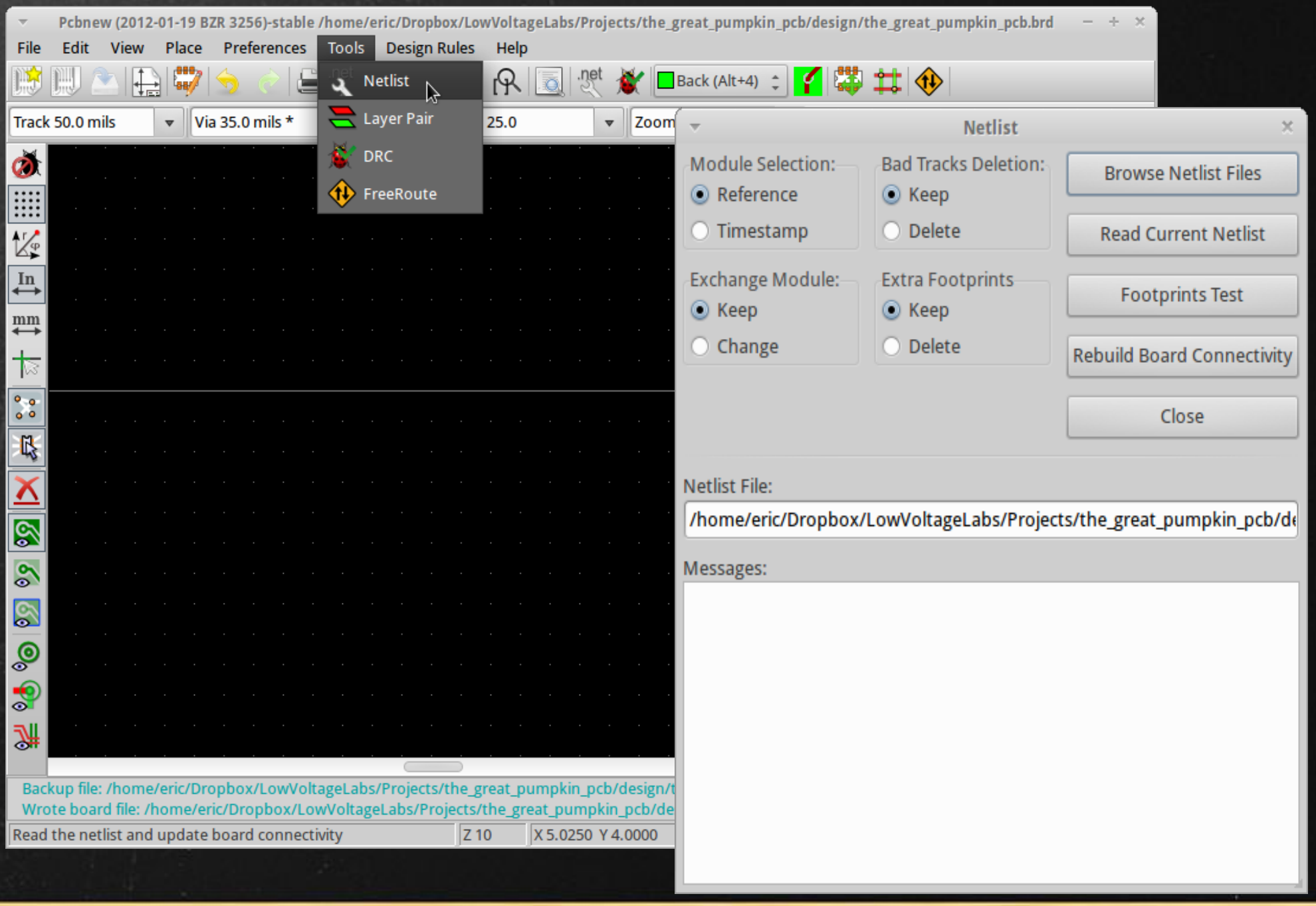
- What is a PCB?
- What is a KiCAD?
- Block diagram
- Schematic
- Schematic attribute editor
- Error check the schematic
- PCB layout
- Error check the layout
- Gerber files
- Build boards

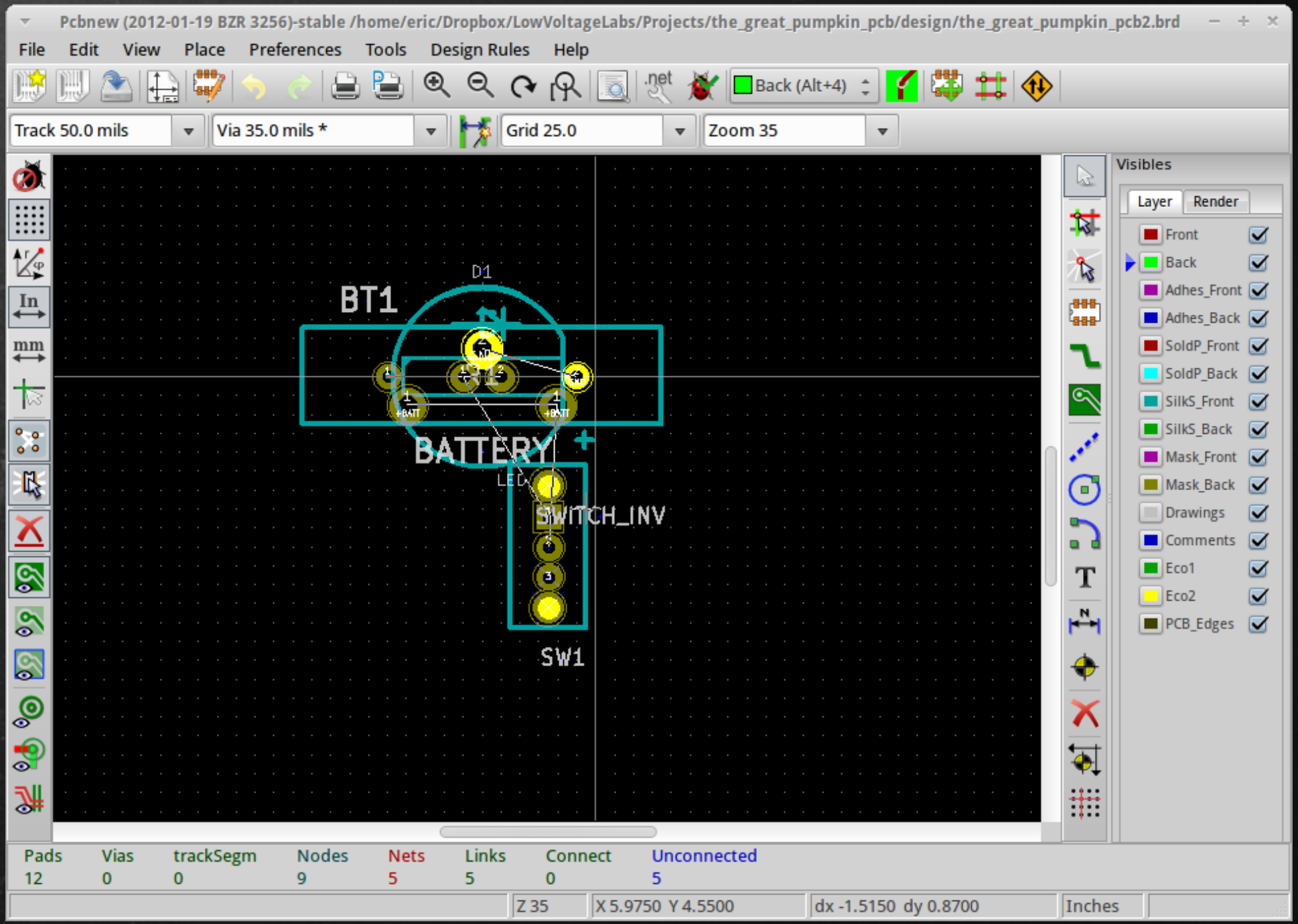

Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.brd
File
Edit
View
Place
Preferences
Tools
Design Rules
Help
Back (Alt+4)
Track 8.0 mils *
Via 35.0 mils *
Grid 2.5
Zoom 50
Visibles
Layer
Render
Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges
Pads
Vias
trackSegm
Nodes
Nets
Links
Connect
Unconnected
0
0
0
0
1
0
0
0
Z 50
X 6.4400 Y 3.4350
dx 6.4400 dy 3.4350
Inches

PCB module editor

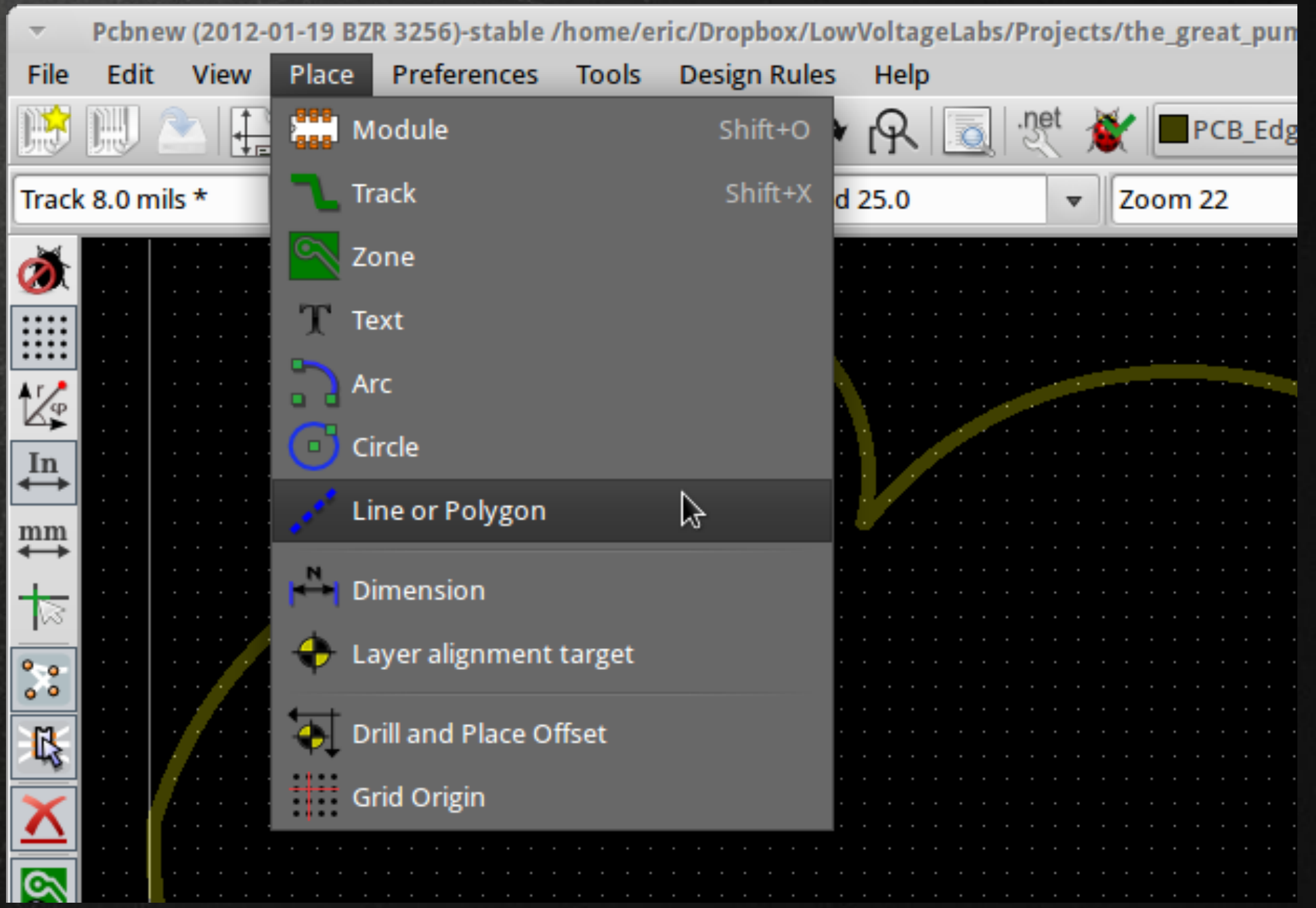


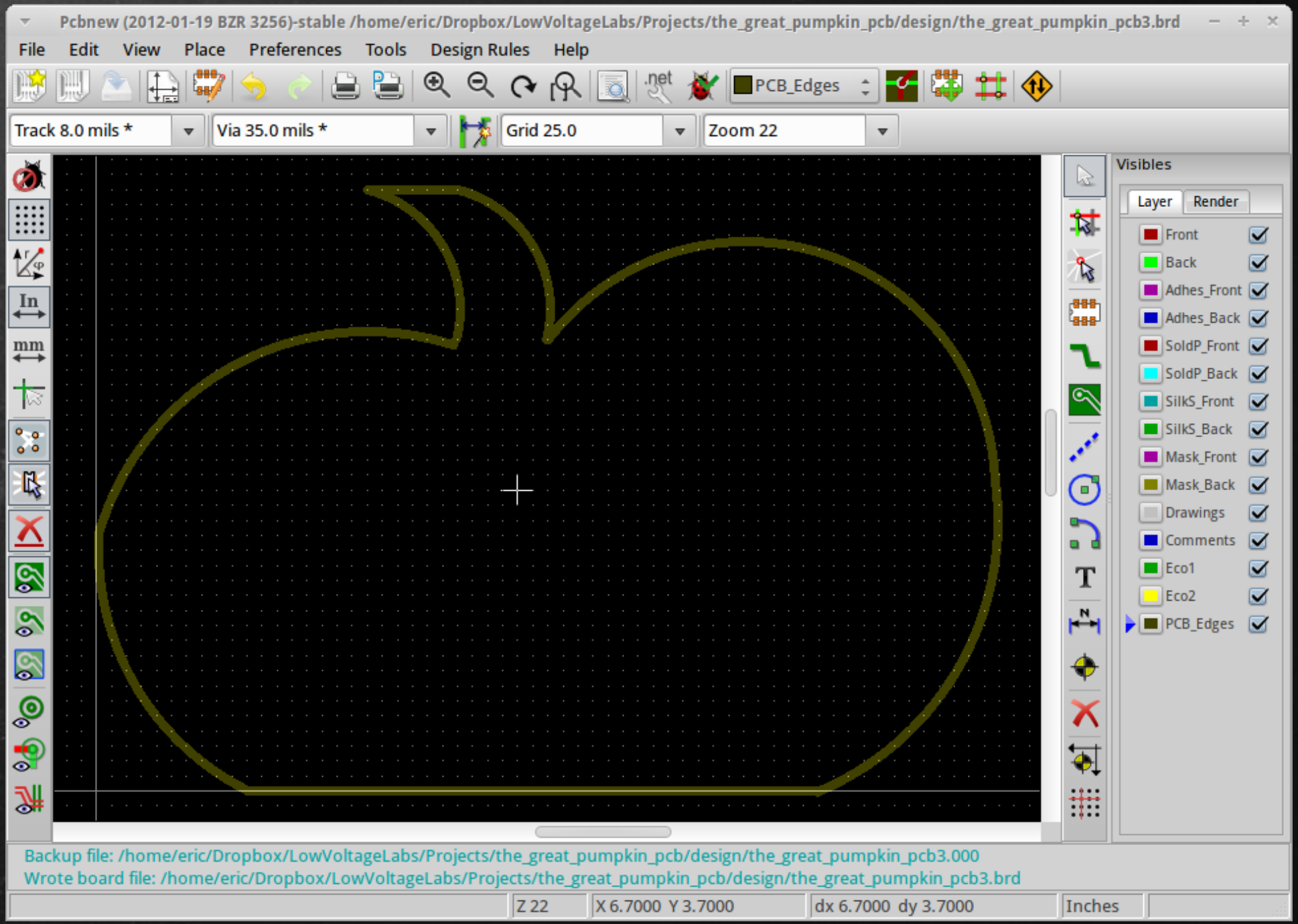
Netlist


Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.brd
File
Edit
View
Place
Preferences
Tools
Design Rules
Help
Netlist
Layer Pair
DRC
FreeRoute
Back (Alt+4)
Track 50.0 mils
Via 35.0 mils *
25.0
Zoom
Netlist
Module Selection:
Reference
Timestamp
Bad Tracks Deletion:
Keep
Delete
Exchange Module:
Keep
Change
Extra Footprints
Keep
Delete
Browse Netlist Files
Read Current Netlist
Footprints Test
Rebuild Board Connectivity
Close
Netlist File:
/home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/de
Messages:
Backup file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/t
Wrote board file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/de
Read the netlist and update board connectivity
Z 10
X 5.0250 Y 4.0000

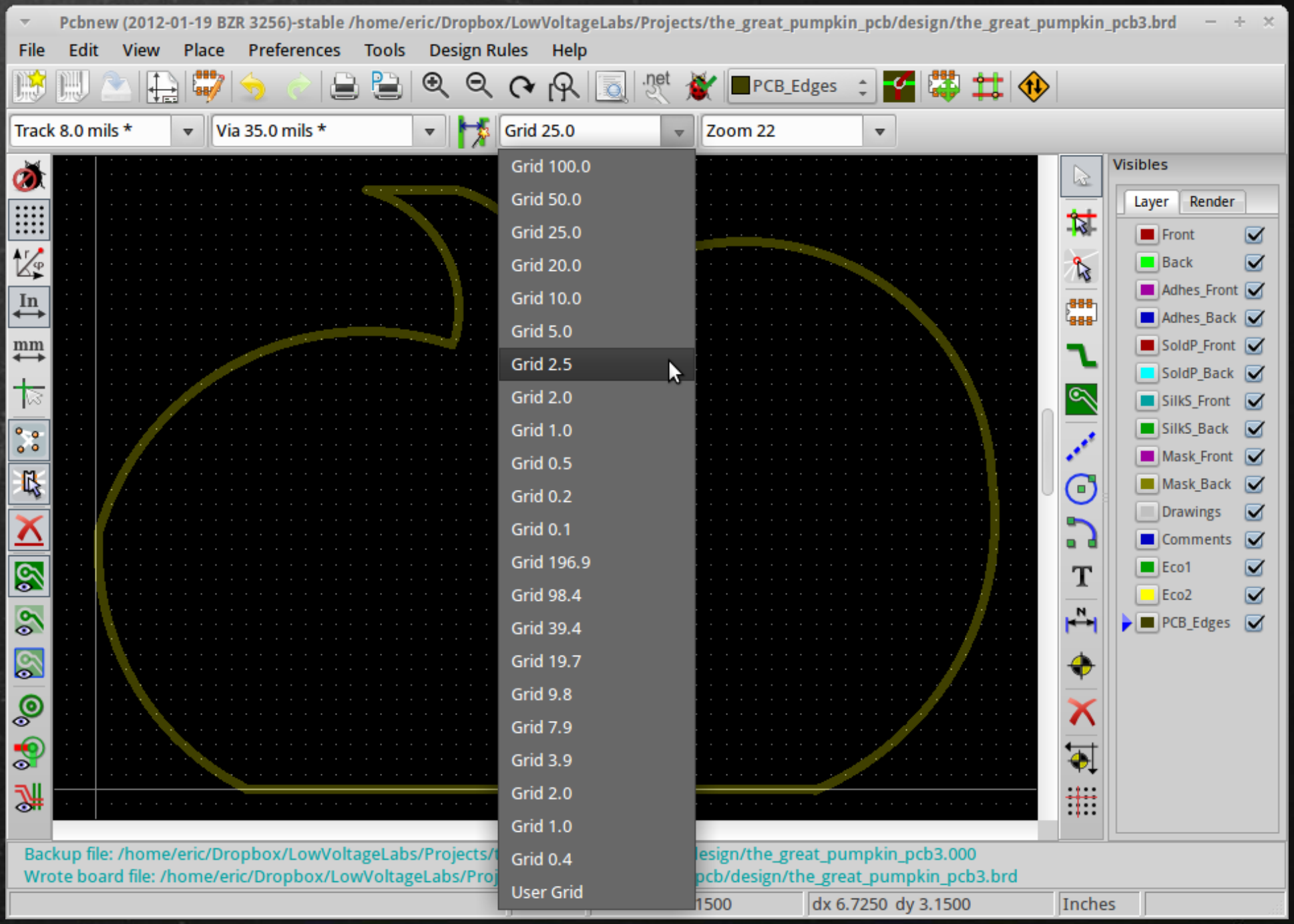

Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb2.brd
File
Edit
View
Place
Preferences
Tools
Design Rules
Help
Back (Alt+4)
Track 50.0 mils
Via 35.0 mils *
Grid 25.0
Zoom 35
D1
BT1
BATTERY
LED
SWITCH_INV
SW1
Visibles
Layer
Render
Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges
Pads
Vias
trackSegm
Nodes
Nets
Links
Connect
Unconnected
12
0
0
9
5
5
0
5
Z 35
X 5.9750 Y 4.5500
dx -1.5150 dy 0.8700
Inches

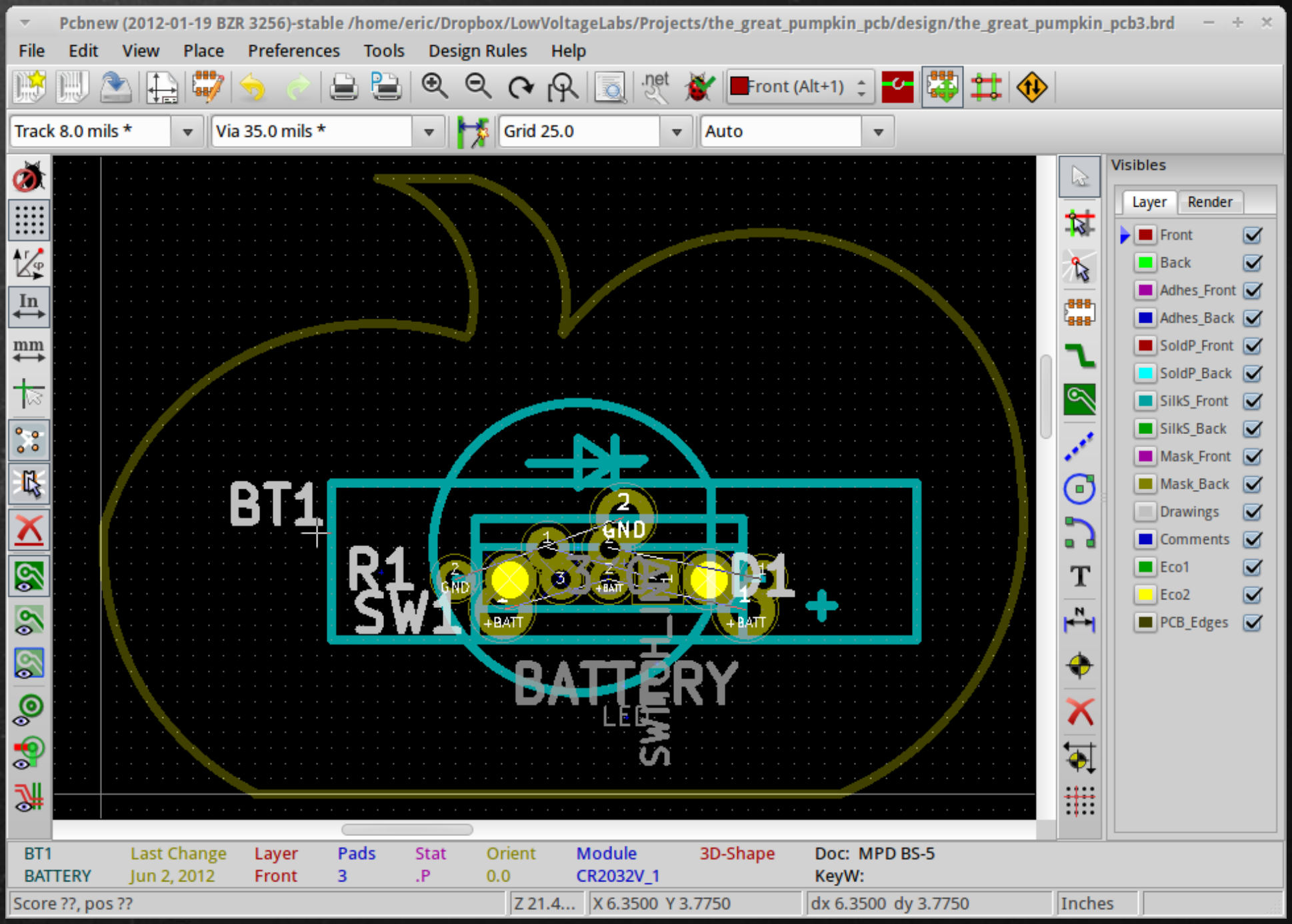
Create an outline on the PCB_Edges layer



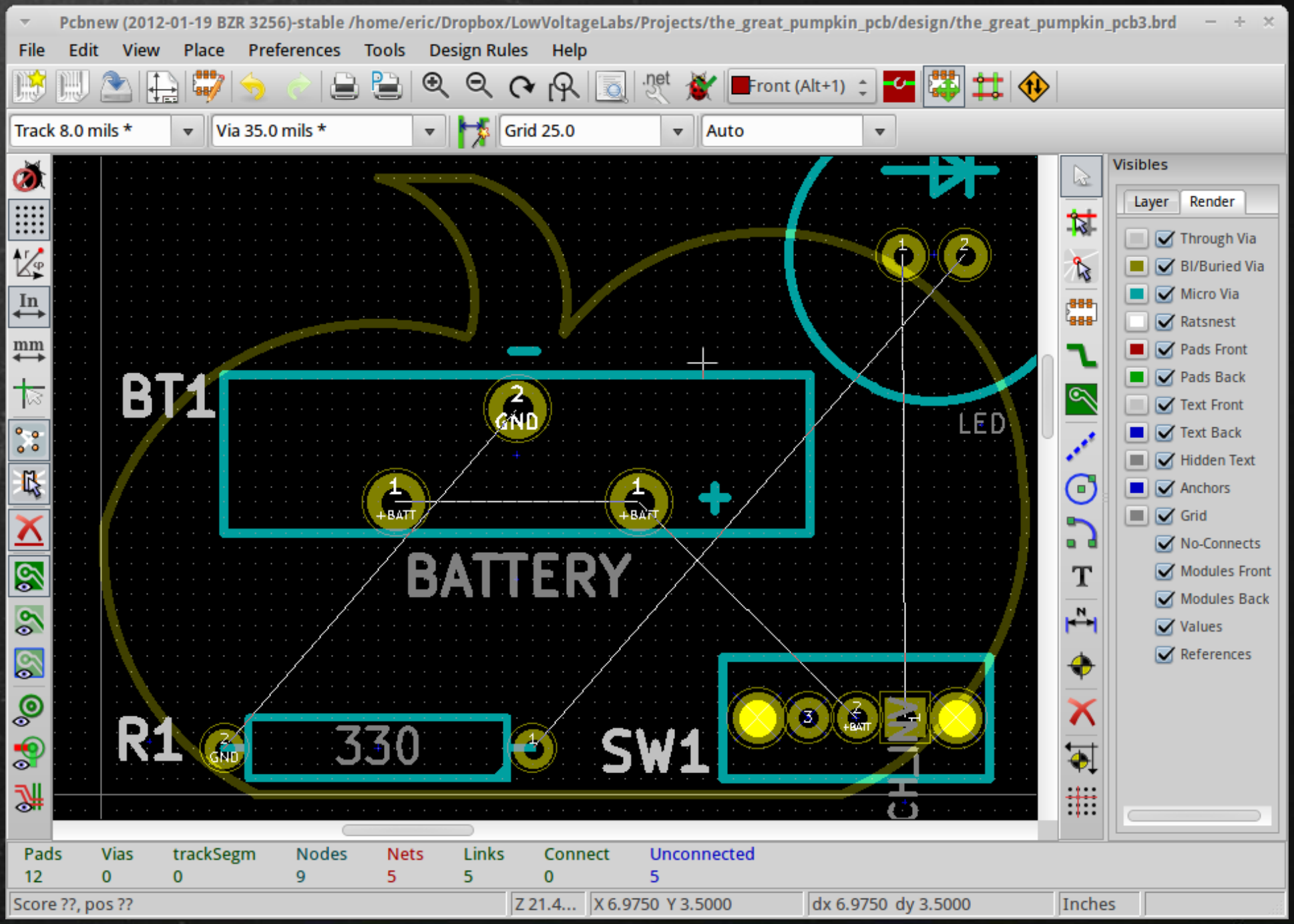

Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb3.brd
File
Edit
View
Place
Preferences
Tools
Design Rules
Help
PCB_Edges
Track 8.0 mils *
Via 35.0 mils *
Grid 25.0
Zoom 22
Visibles
Layer
Render
Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges
Backup file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb3.000
Wrote board file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb3.brd
Z 22
X 6.7000 Y 3.7000
dx 6.7000 dy 3.7000
Inches

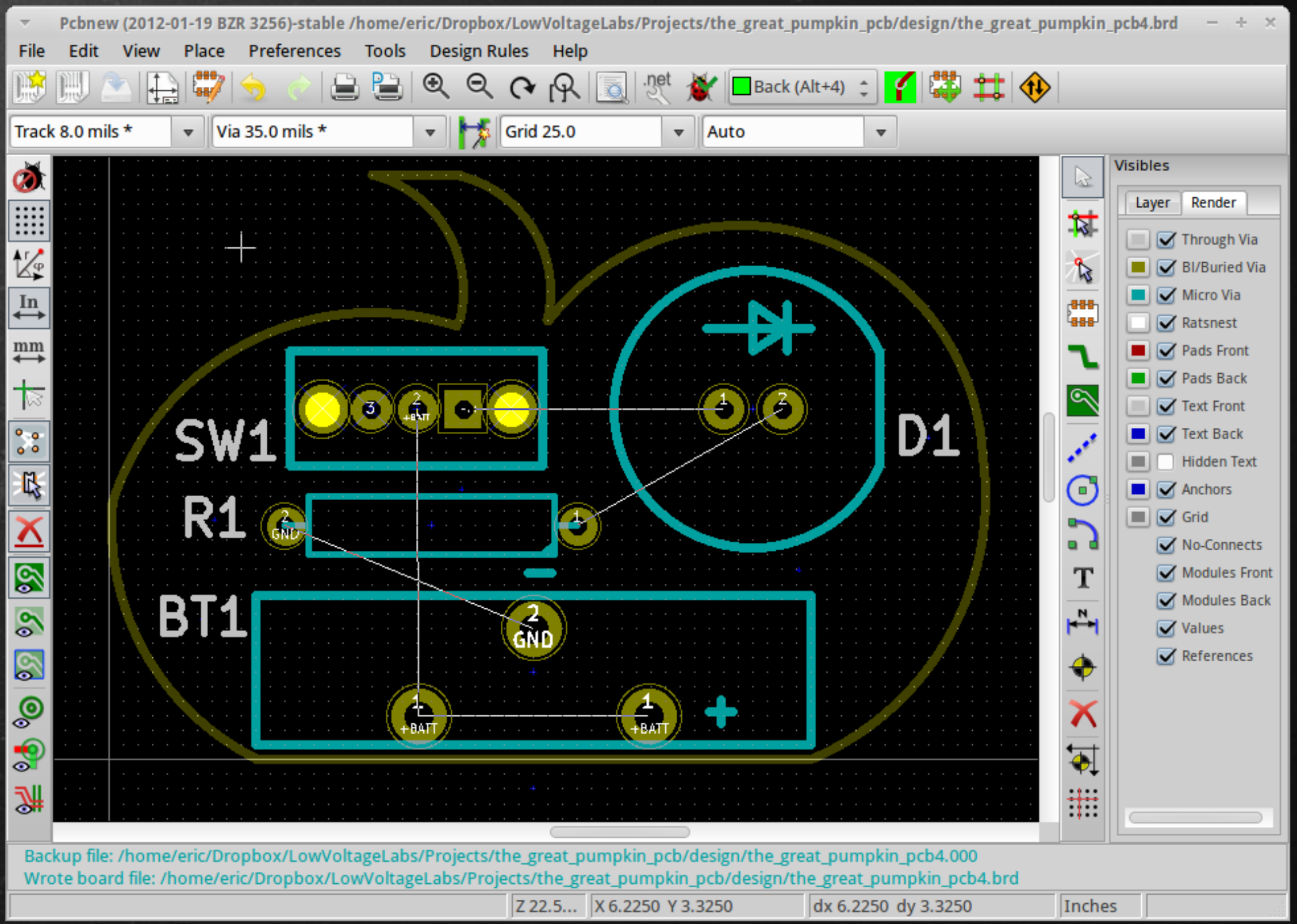
Grid


Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb3.brd
File
Edit
View
Place
Preferences
Tools
Design Rules
Help
PCB_Edges
Track 8.0 mils *
Via 35.0 mils *
Grid 25.0
Zoom 22
Grid 100.0
Grid 50.0
Grid 25.0
Grid 20.0
Grid 10.0
Grid 5.0
Grid 2.5
Grid 2.0
Grid 1.0
Grid 0.5
Grid 0.2
Grid 0.1
Grid 196.9
Grid 98.4
Grid 39.4
Grid 19.7
Grid 9.8
Grid 7.9
Grid 3.9
Grid 2.0
Grid 1.0
Grid 0.4
User Grid
Visibles
Layer
Render
Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges
Backup file: /home/eric/Dropbox/LowVoltageLabs/Projects/
esign/the_great_pumpkin_pcb3.000
Wrote board file: /home/eric/Dropbox/LowVoltageLabs/Proj
pcb/design/the_great_pumpkin_pcb3.brd
1500
dx 6.7250 dy 3.1500
Inches

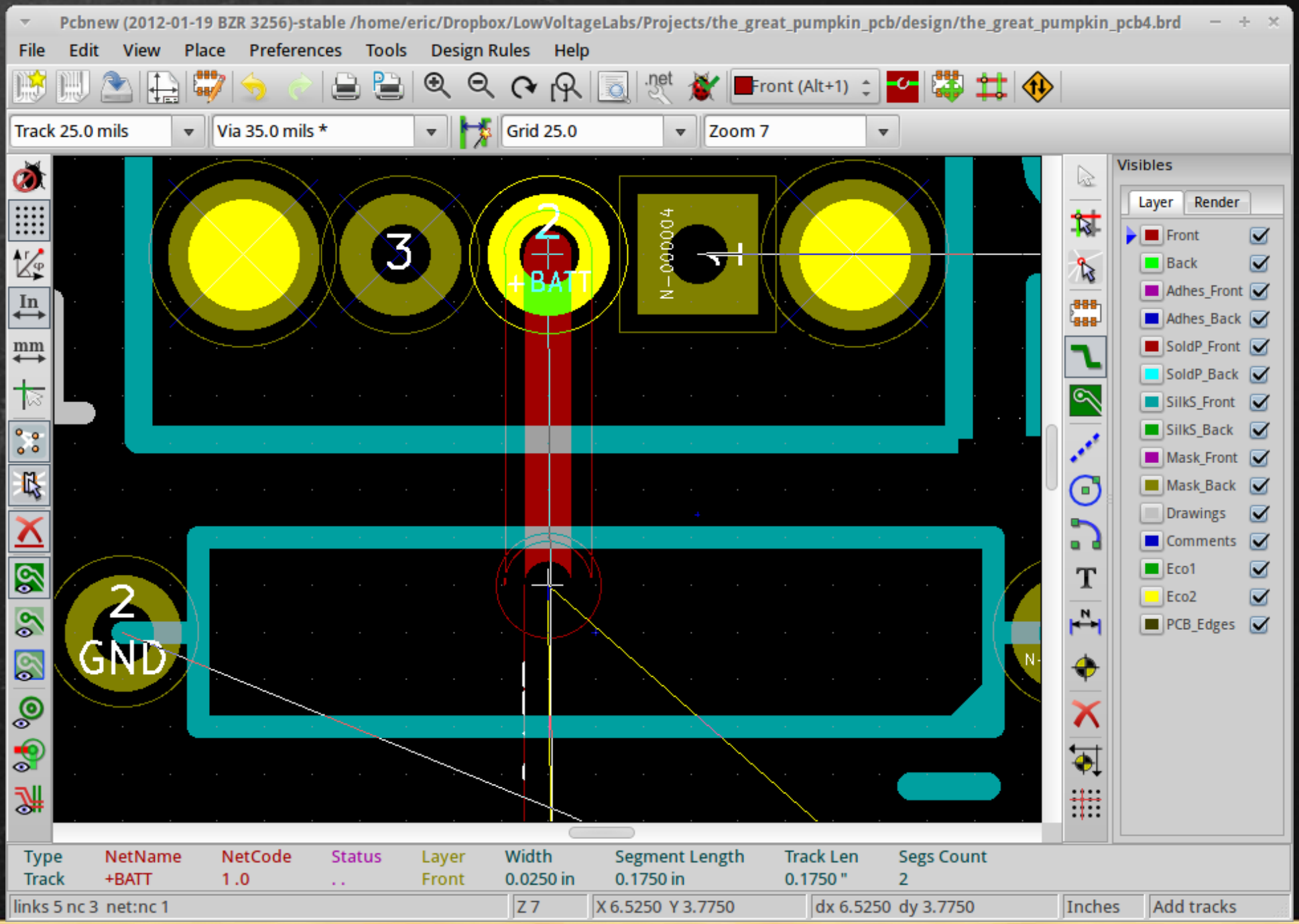

Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb3.brd
File Edit View Place Preferences Tools Design Rules Help
Front (Alt+1)
Track 8.0 mils *
Via 35.0 mils *
Grid 25.0
Auto
Visibles
Layer Render
Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges
BT1
R1
SW1
GND
+BATT
BATTERY
BT1 BATTERY
Last Change Jun 2, 2012
Layer Front
Pads 3
Stat .P
Orient 0.0
Module CR2032V_1
3D-Shape
Doc: MPD BS-5
KeyW:
Score ??, pos ??
Z 21.4...
X 6.3500 Y 3.7750
dx 6.3500 dy 3.7750
Inches

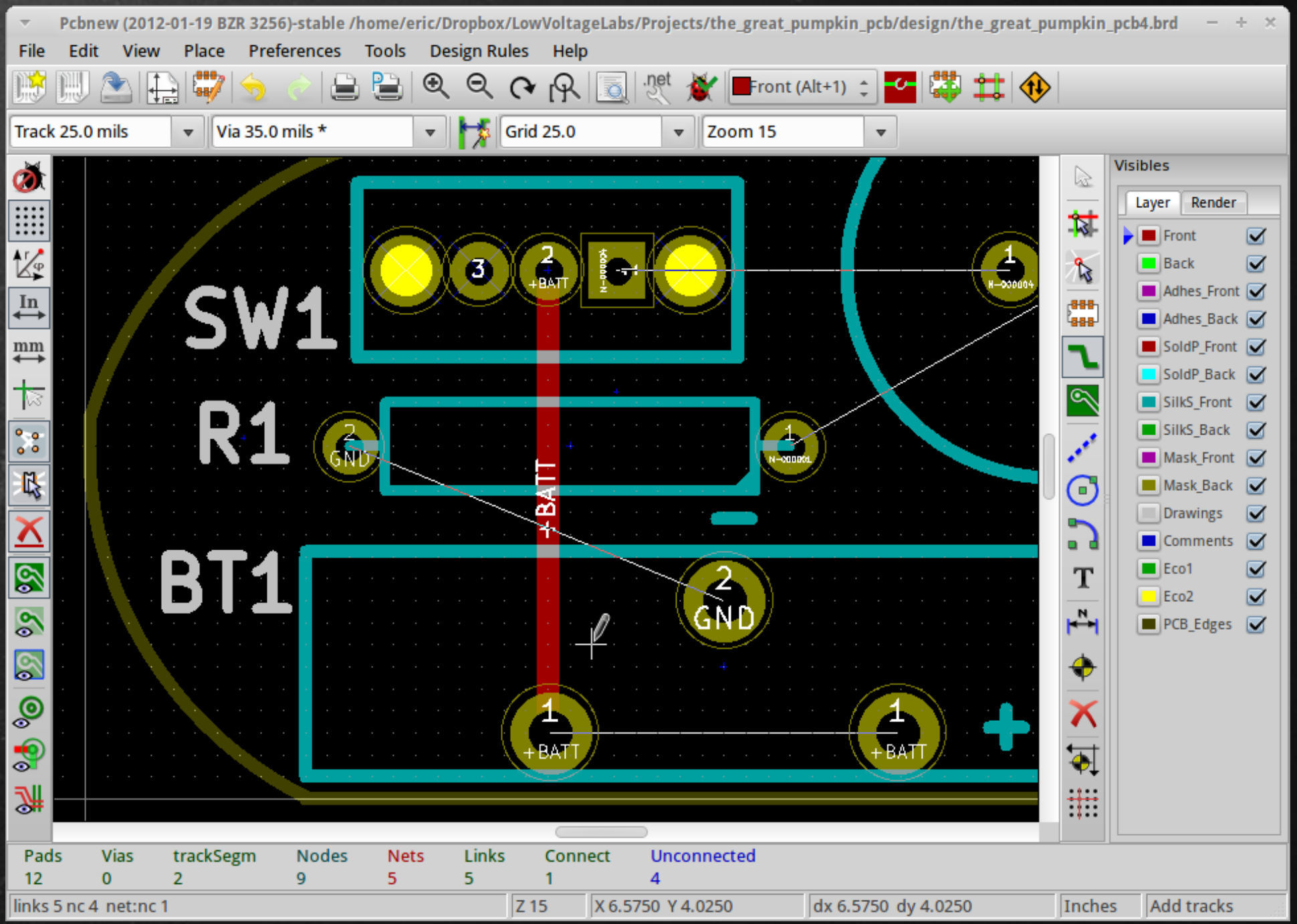
'm' to move parts, ratsnests to help determine locations



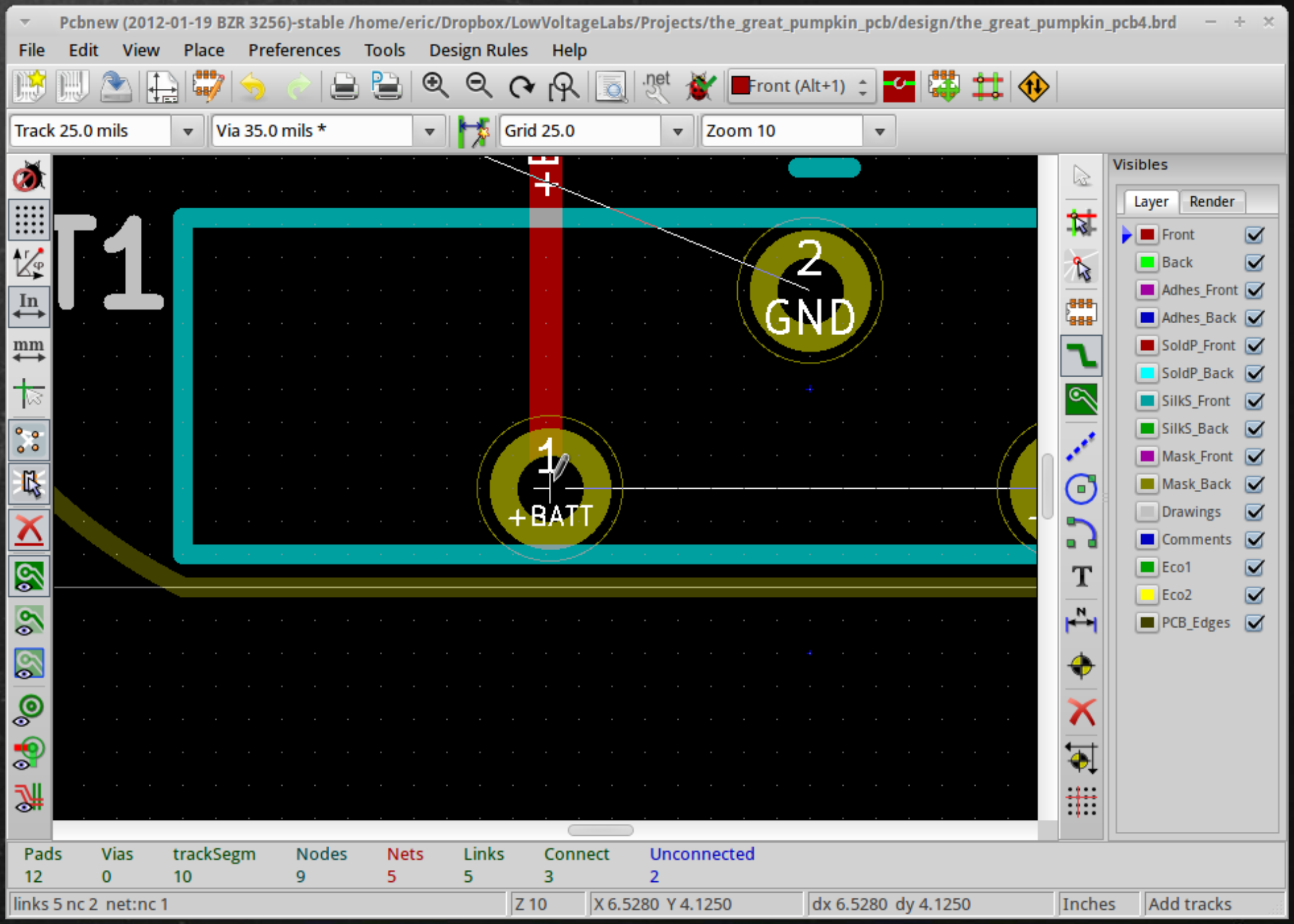

Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb4.brd
File
Edit
View
Place
Preferences
Tools
Design Rules
Help
Back (Alt+4)
Track 8.0 mils *
Via 35.0 mils *
Grid 25.0
Auto
SW1
D1
R1
BT1
GND
+BATT
Visibles
Layer
Render
Through Via
Bl/Buried Via
Micro Via
Ratsnest
Pads Front
Pads Back
Text Front
Text Back
Hidden Text
Anchors
Grid
No-Connects
Modules Front
Modules Back
Values
References
Backup file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb4.000
Wrote board file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb4.brd
Z 22.5...
X 6.2250 Y 3.3250
dx 6.2250 dy 3.3250
Inches

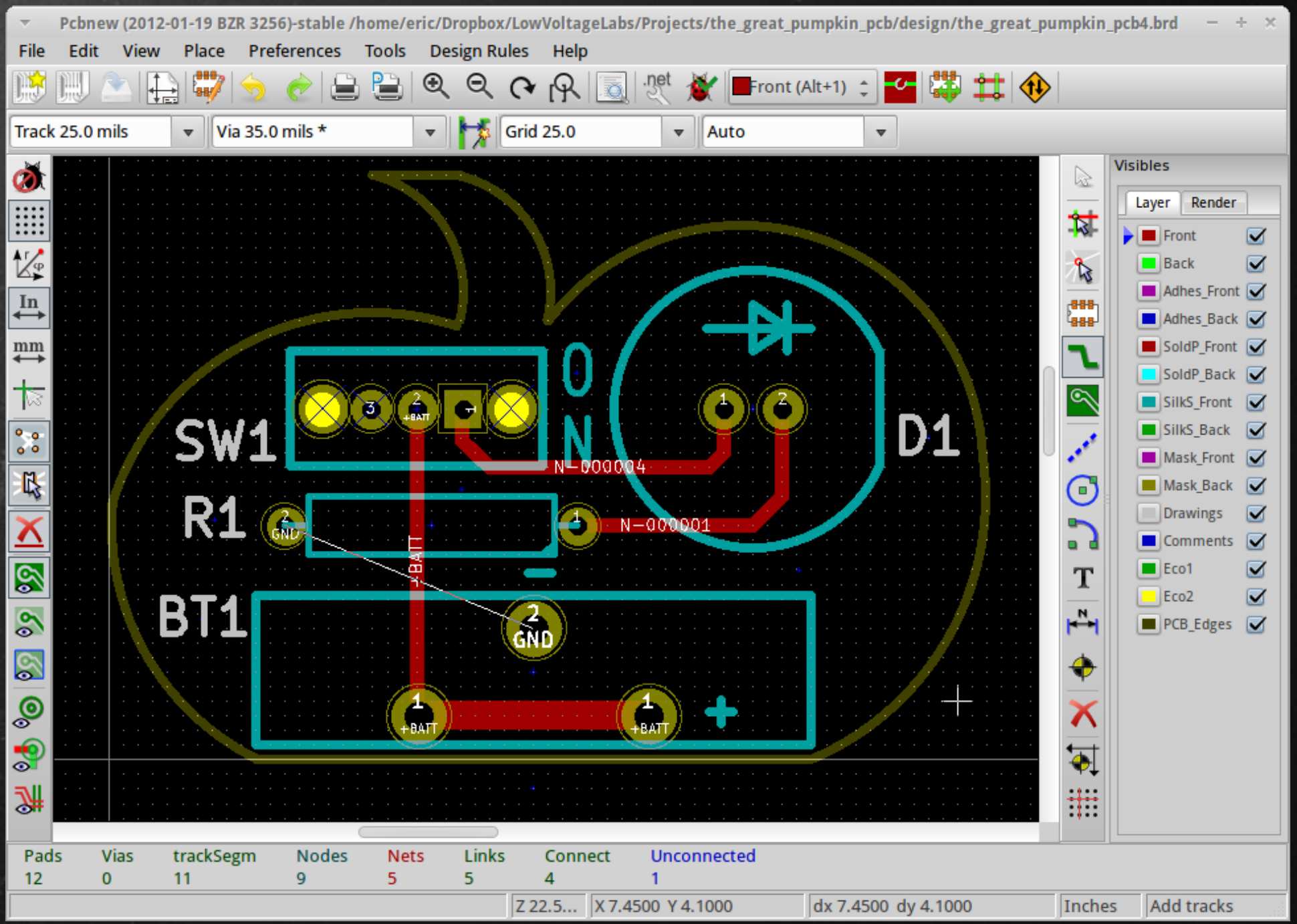
Place a track with shift-x

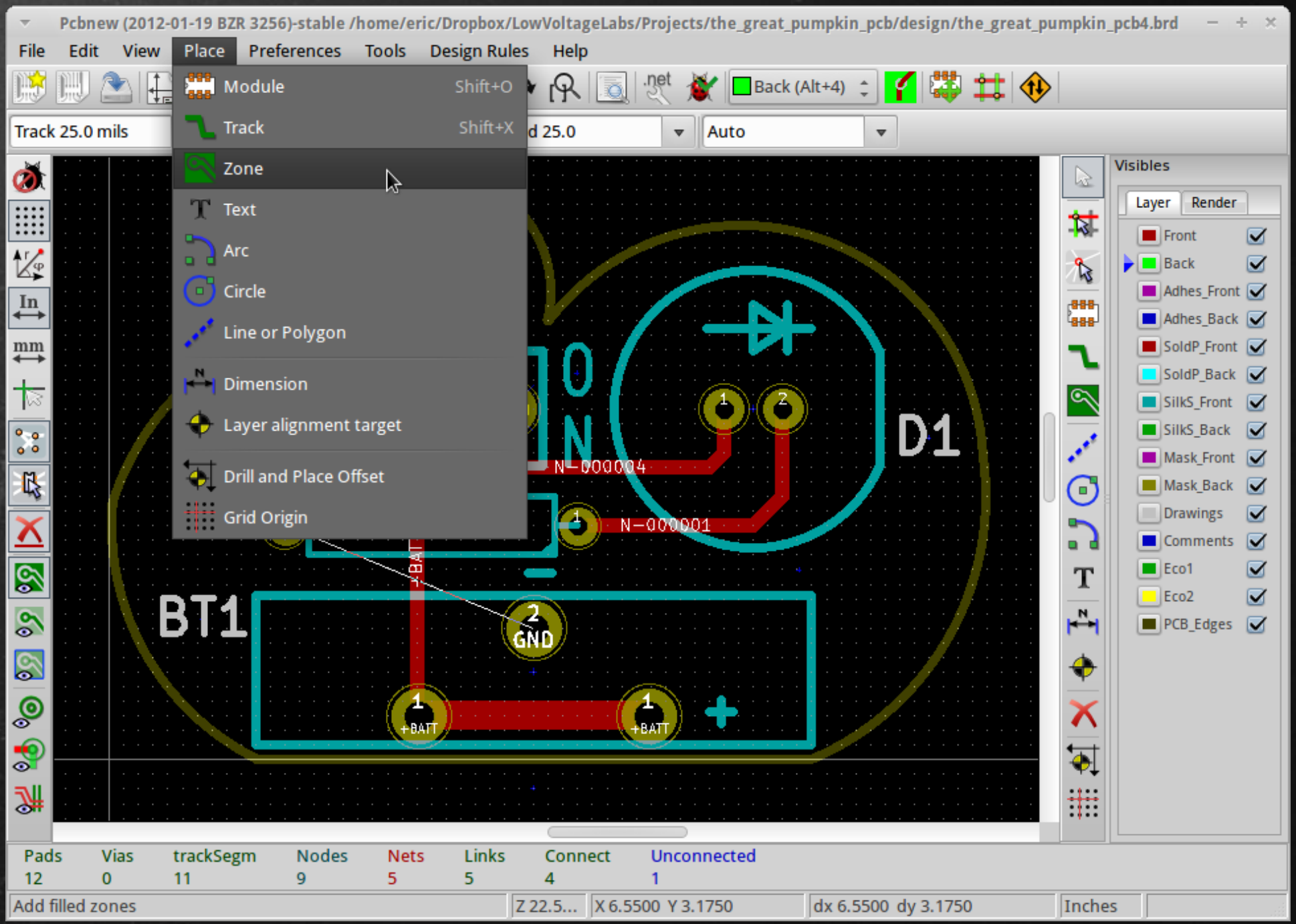


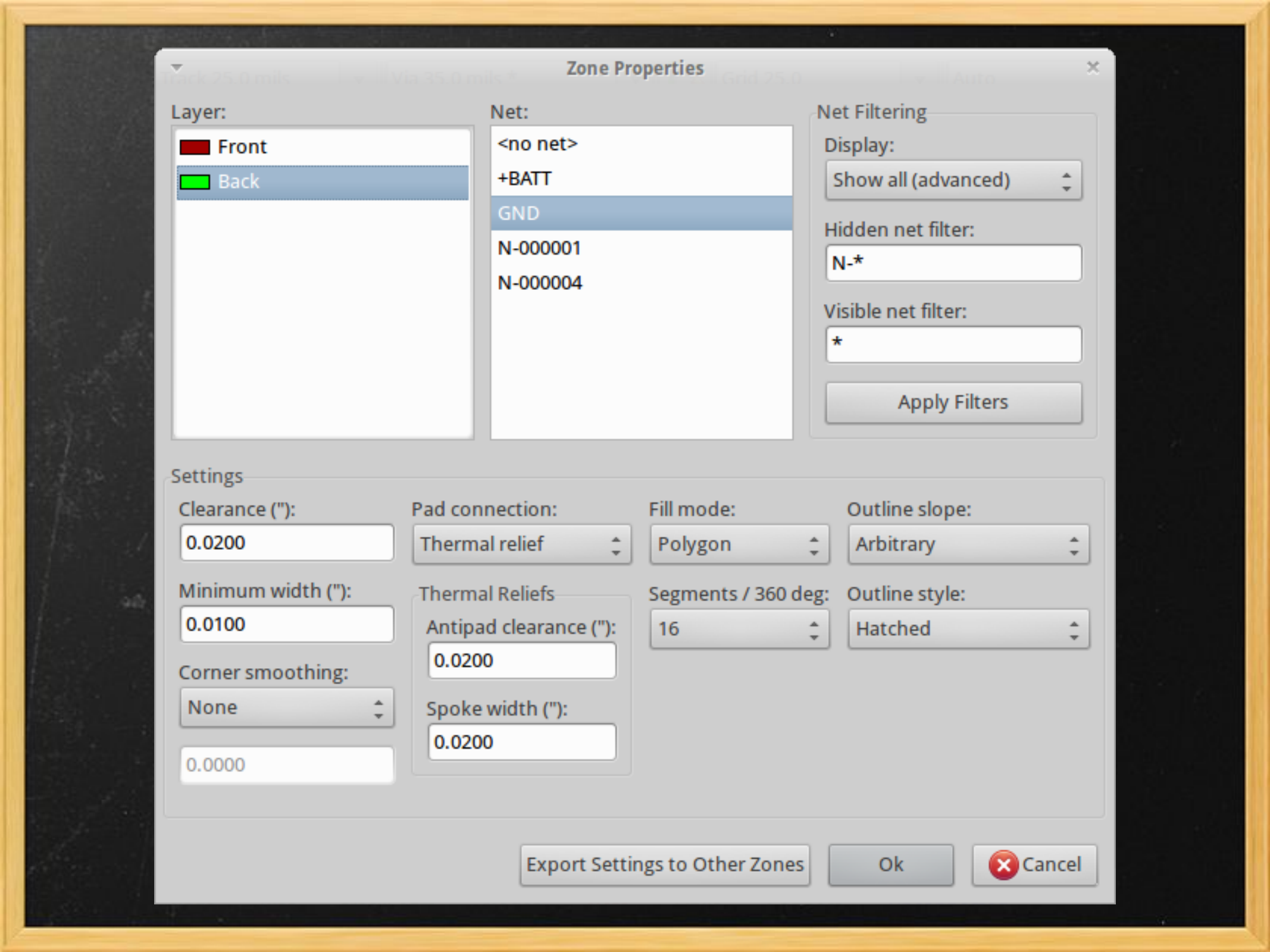

Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb4.brd
File
Edit
View
Place
Preferences
Tools
Design Rules
Help
Front (Alt+1)
Track 25.0 mils
Via 35.0 mils *
Grid 25.0
Zoom 15
SW1
R1
BT1
+BATT
GND
Visibles
Layer
Render
Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges
Pads
Vias
trackSegm
Nodes
Nets
Links
Connect
Unconnected
12
0
2
9
5
5
1
4
links 5 nc 4 net:nc 1
Z 15
X 6.5750 Y 4.0250
dx 6.5750 dy 4.0250
Inches
Add tracks

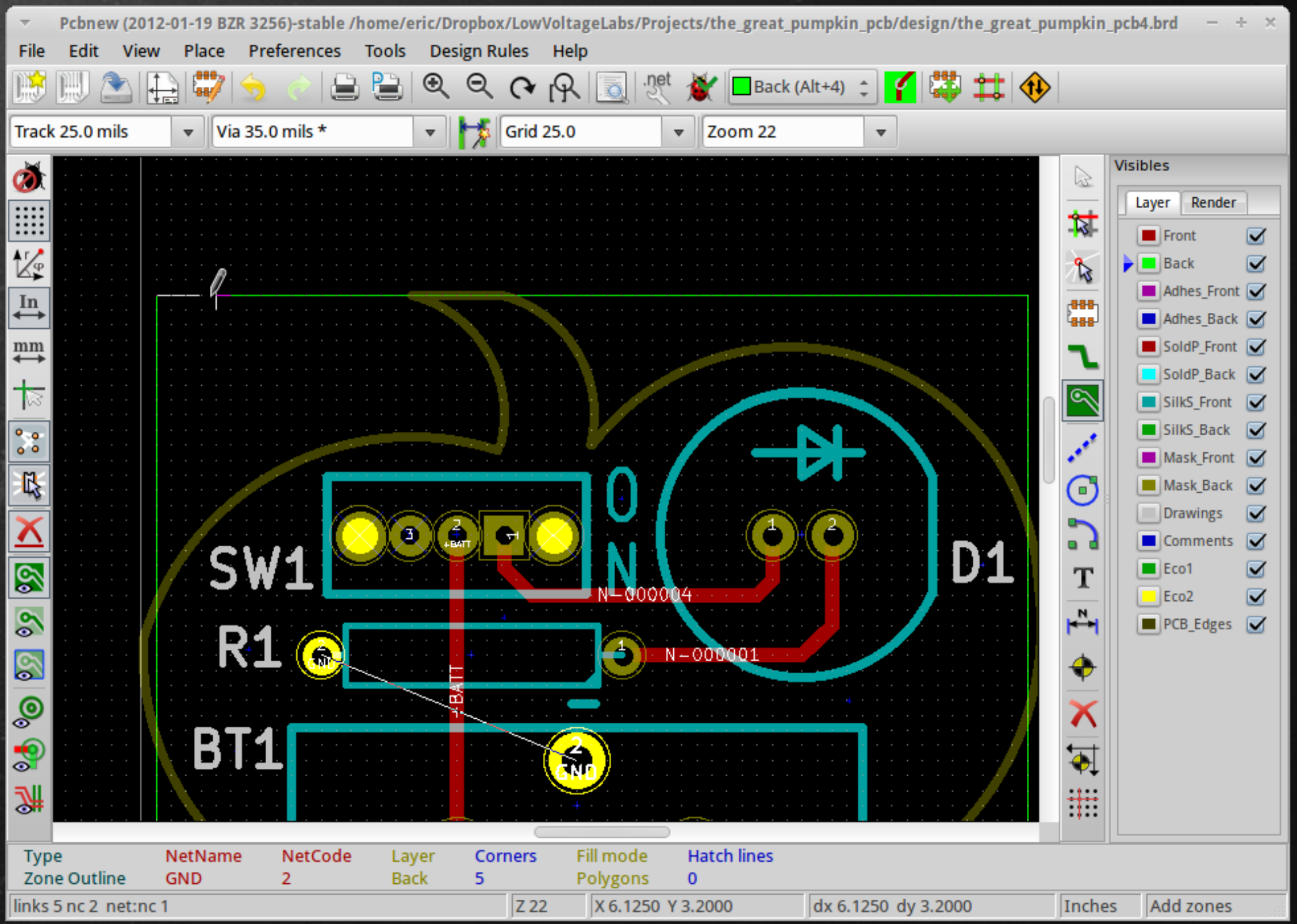
Double click to end the track at the battery

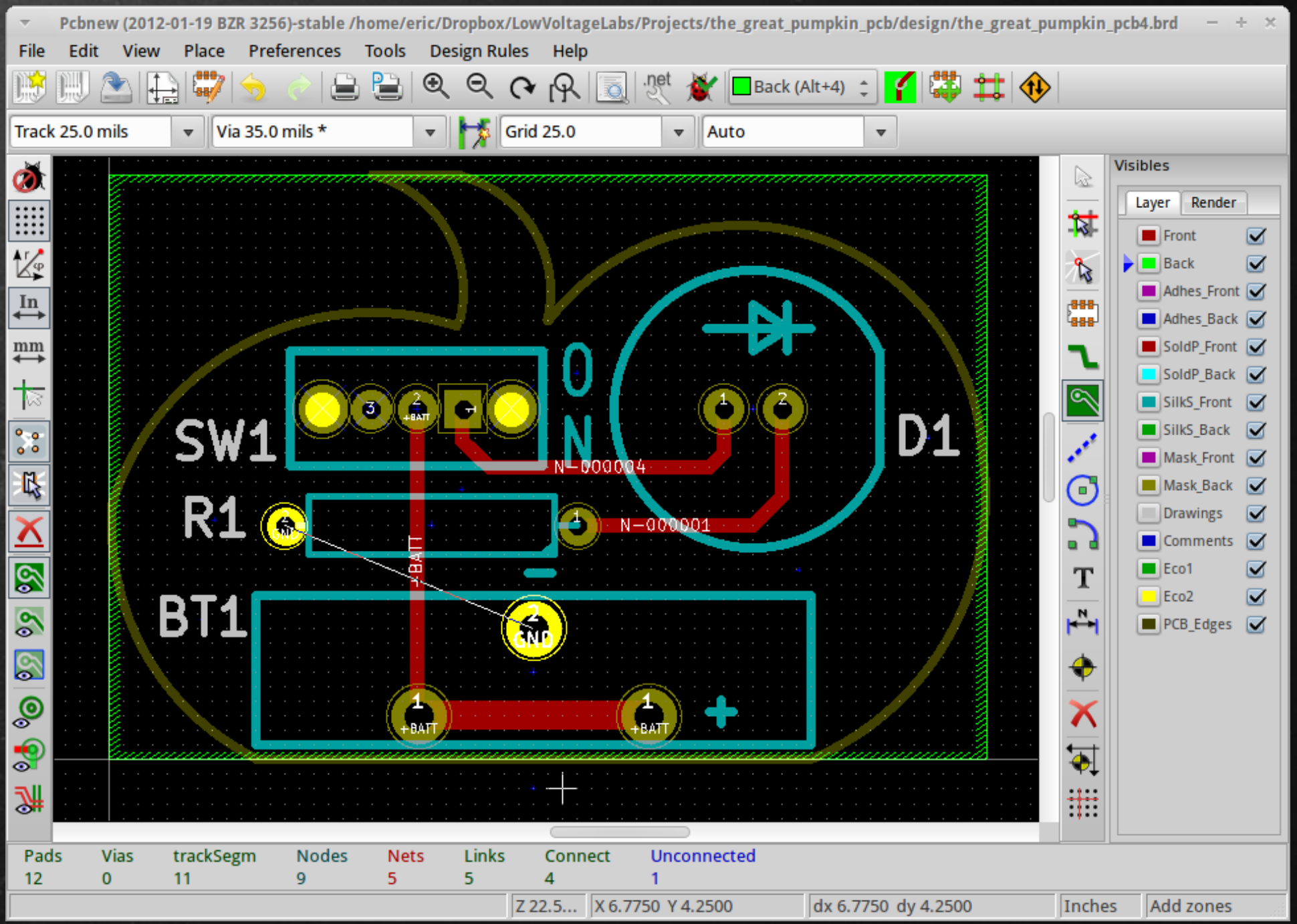



Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb4.brd
File
Edit
View
Place
Preferences
Tools
Design Rules
Help
Front (Alt+1)
Track 25.0 mils
Via 35.0 mils *
Grid 25.0
Auto
Visibles
Layer
Render
Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges
SW1
ON
D1
R1
BT1
N-000004
N-000001
-BATT
GND
+BATT
Pads
Vias
trackSegm
Nodes
Nets
Links
Connect
Unconnected
12
0
11
9
5
5
4
1
Z 22.5...
X 7.4500 Y 4.1000
dx 7.4500 dy 4.1000
Inches
Add tracks

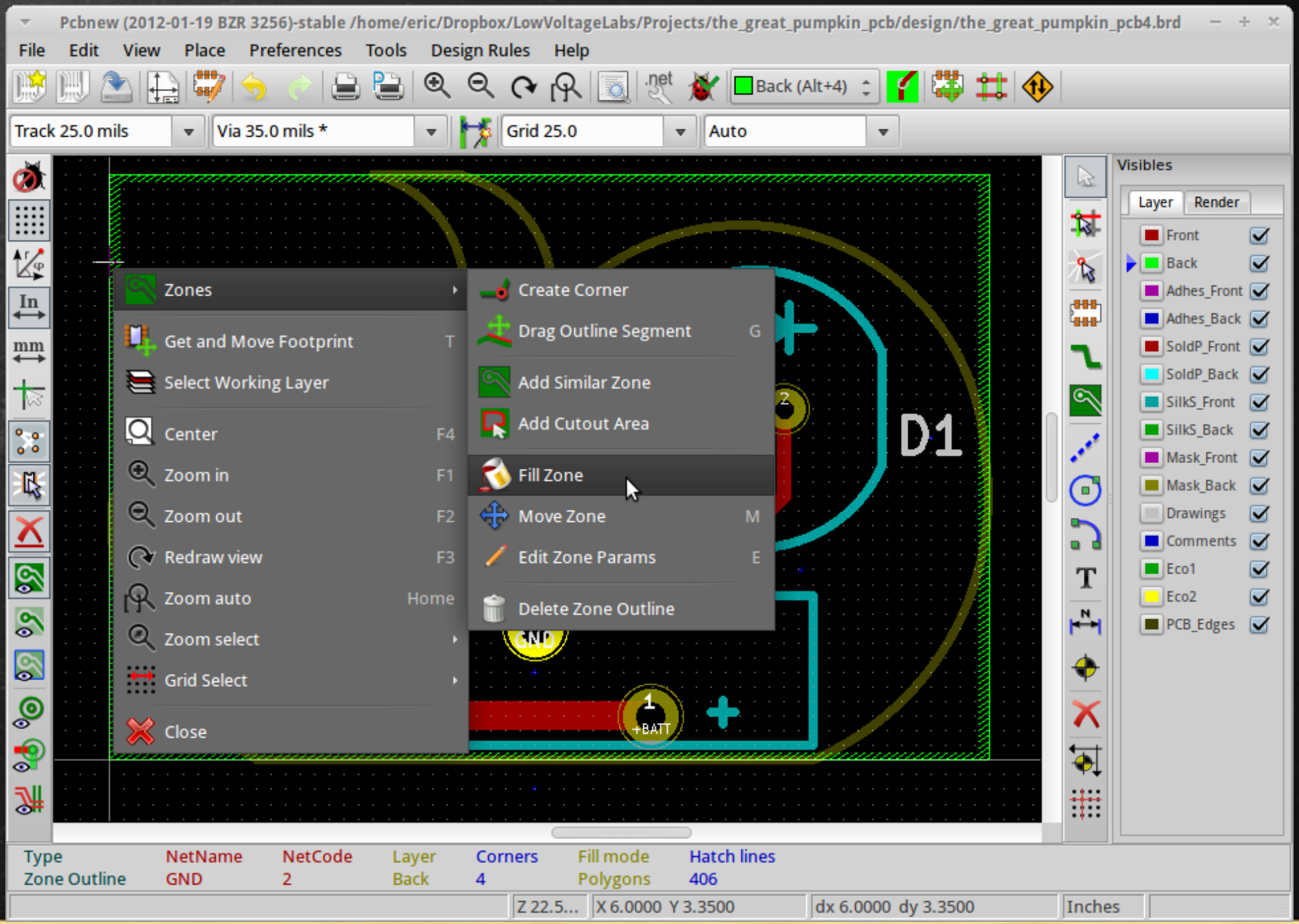

Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb4.brd
File
Edit
View
Place
Preferences
Tools
Design Rules
Help
Module Shift+O
Track Shift+X
Zone
Text
Arc
Circle
Line or Polygon
Dimension
Layer alignment target
Drill and Place Offset
Grid Origin
Back (Alt+4)
Track 25.0 mils
Auto
Visibles
Layer
Render
Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges
D1
BT1
N-000004
N-000001
GND
+BATT
Pads 12
Vias 0
trackSegm 11
Nodes 9
Nets 5
Links 5
Connect 4
Unconnected 1
Add filled zones
Z 22.5...
X 6.5500 Y 3.1750
dx 6.5500 dy 3.1750
Inches

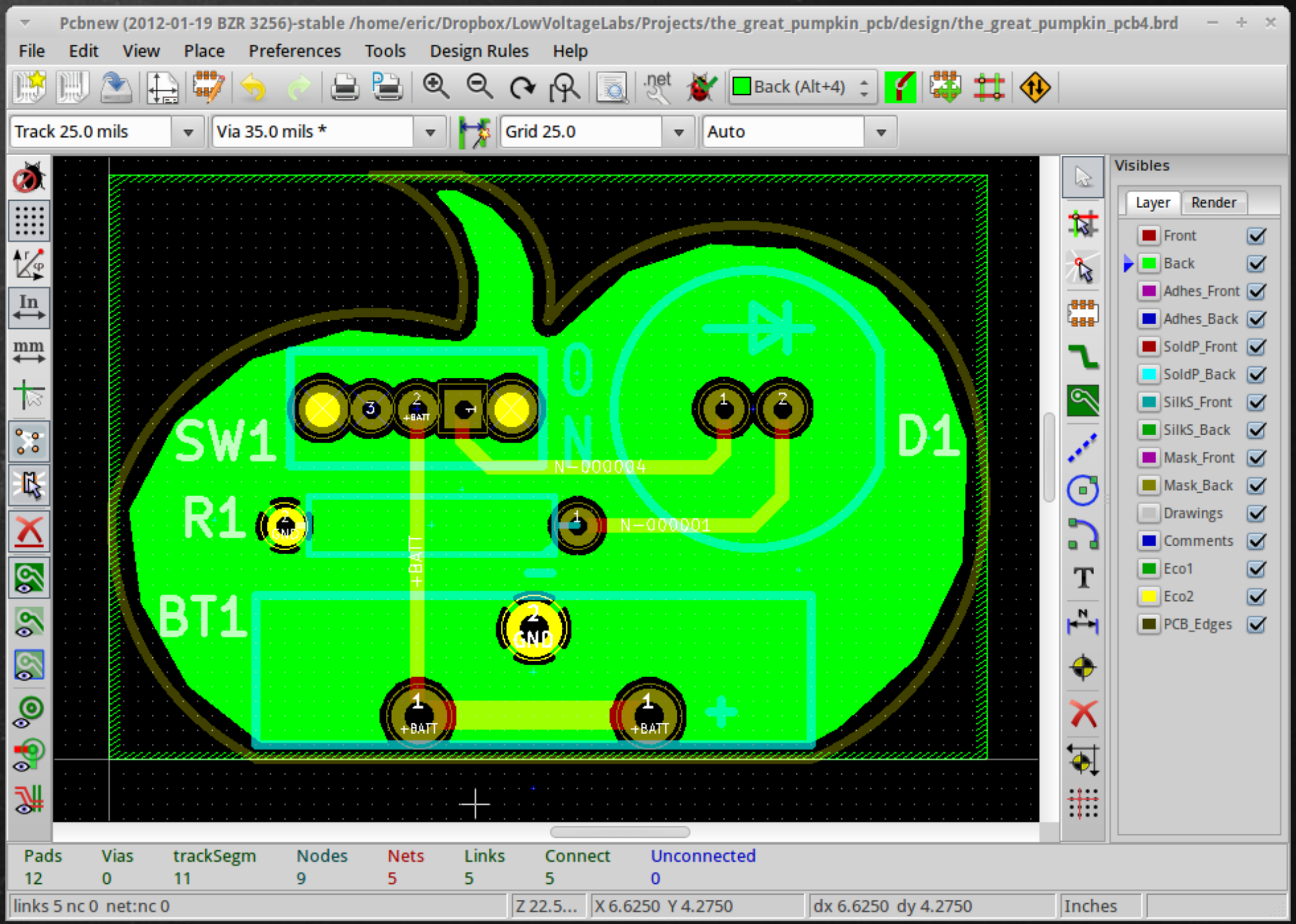

Zone Properties
Layer:
Front
Back
Net:
<no net>
+BATT
GND
N-000001
N-000004
Net Filtering
Display:
Show all (advanced)
Hidden net filter:
N-*
Visible net filter:
*
Apply Filters
Settings
Clearance ("):
0.0200
Pad connection:
Thermal relief
Fill mode:
Polygon
Outline slope:
Arbitrary
Minimum width ("):
0.0100
Thermal Reliefs
Antipad clearance ("):
0.0200
Segments / 360 deg:
16
Outline style:
Hatched
Corner smoothing:
None
Spoke width ("):
0.0200
0.0000
Export Settings to Other Zones
Ok
Cancel


Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb4.brd
File Edit View Place Preferences Tools Design Rules Help
Back (Alt+4)
Track 25.0 mils
Via 35.0 mils *
Grid 25.0
Zoom 22
Visibles
Layer Render
Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges
SW1
R1
BT1
D1
ON
N-000004
N-000001
+BATT
GND
Type NetName NetCode Layer Corners Fill mode Hatch lines
Zone Outline GND 2 Back 5 Polygons 0
links 5 nc 2 net:nc 1
Z 22
X 6.1250 Y 3.2000
dx 6.1250 dy 3.2000
Inches
Add zones

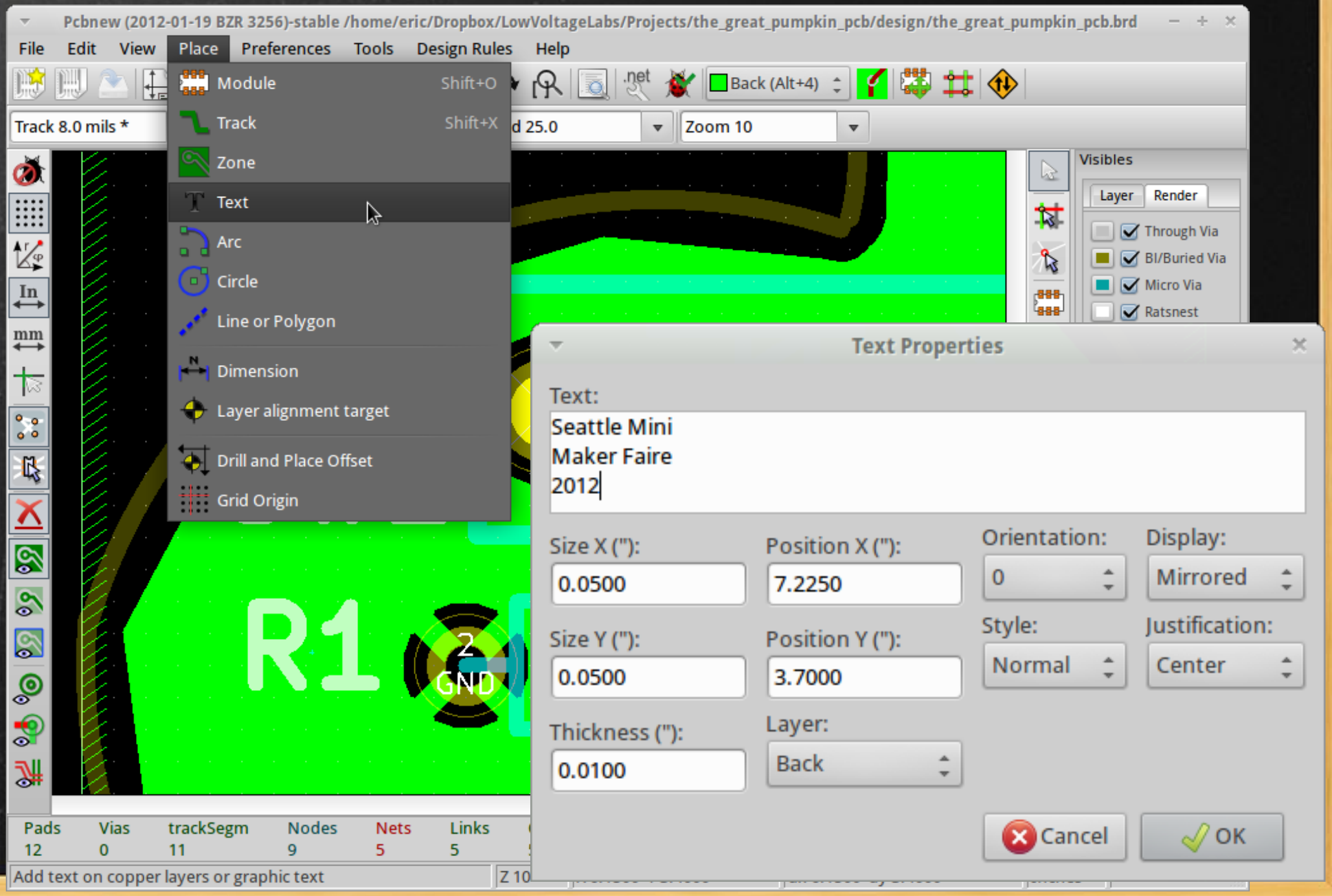

Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb4.brd
File
Edit
View
Place
Preferences
Tools
Design Rules
Help
Back (Alt+4)
Track 25.0 mils
Via 35.0 mils *
Grid 25.0
Auto
Visibles
Layer
Render
Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges
SW1
ON
D1
R1
BT1
N-000004
N-000001
-BATT
+BATT
GND
Pads
Vias
trackSegm
Nodes
Nets
Links
Connect
Unconnected
12
0
11
9
5
5
4
1
Z 22.5...
X 6.7750 Y 4.2500
dx 6.7750 dy 4.2500
Inches
Add zones

Right click on the zone

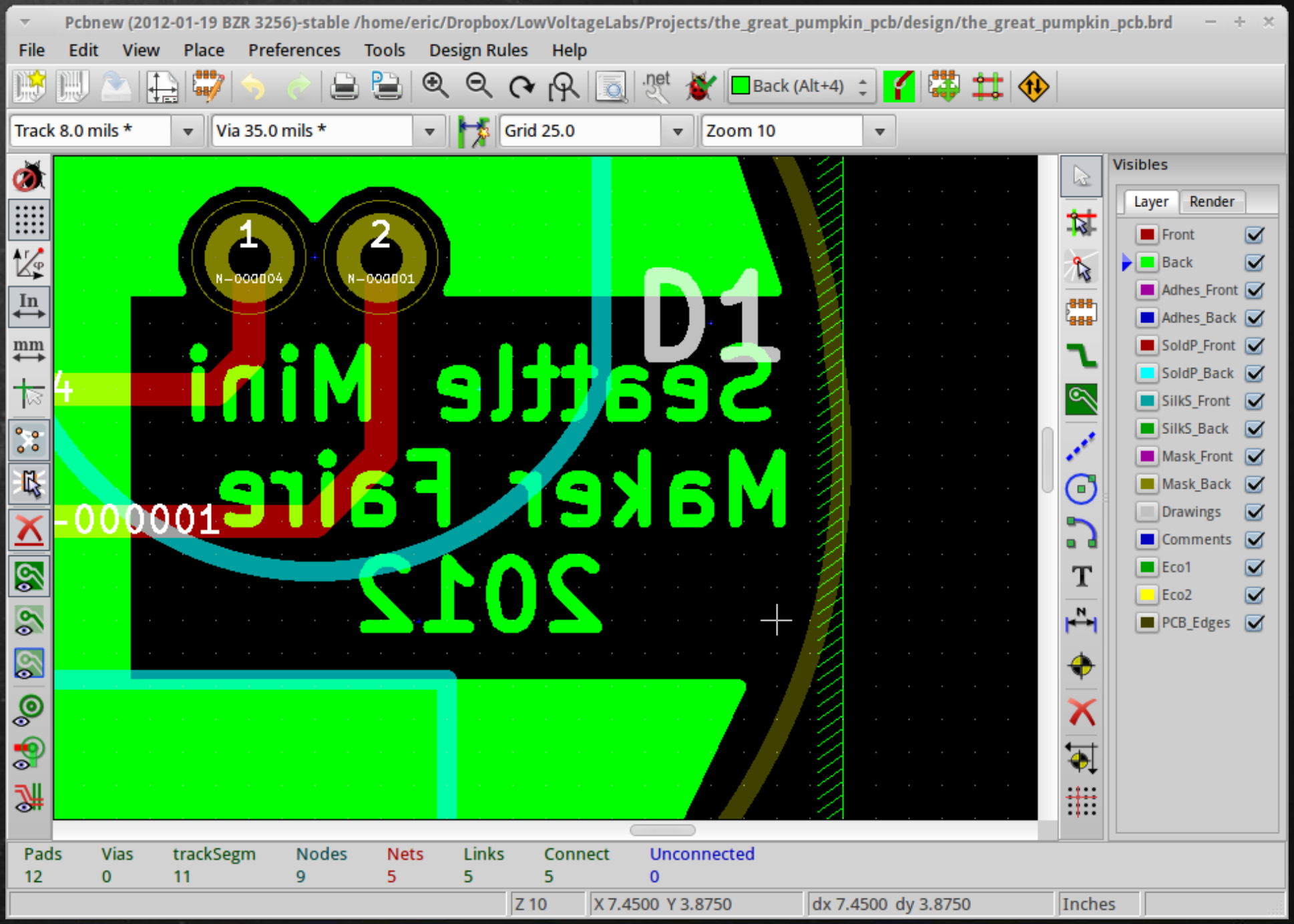


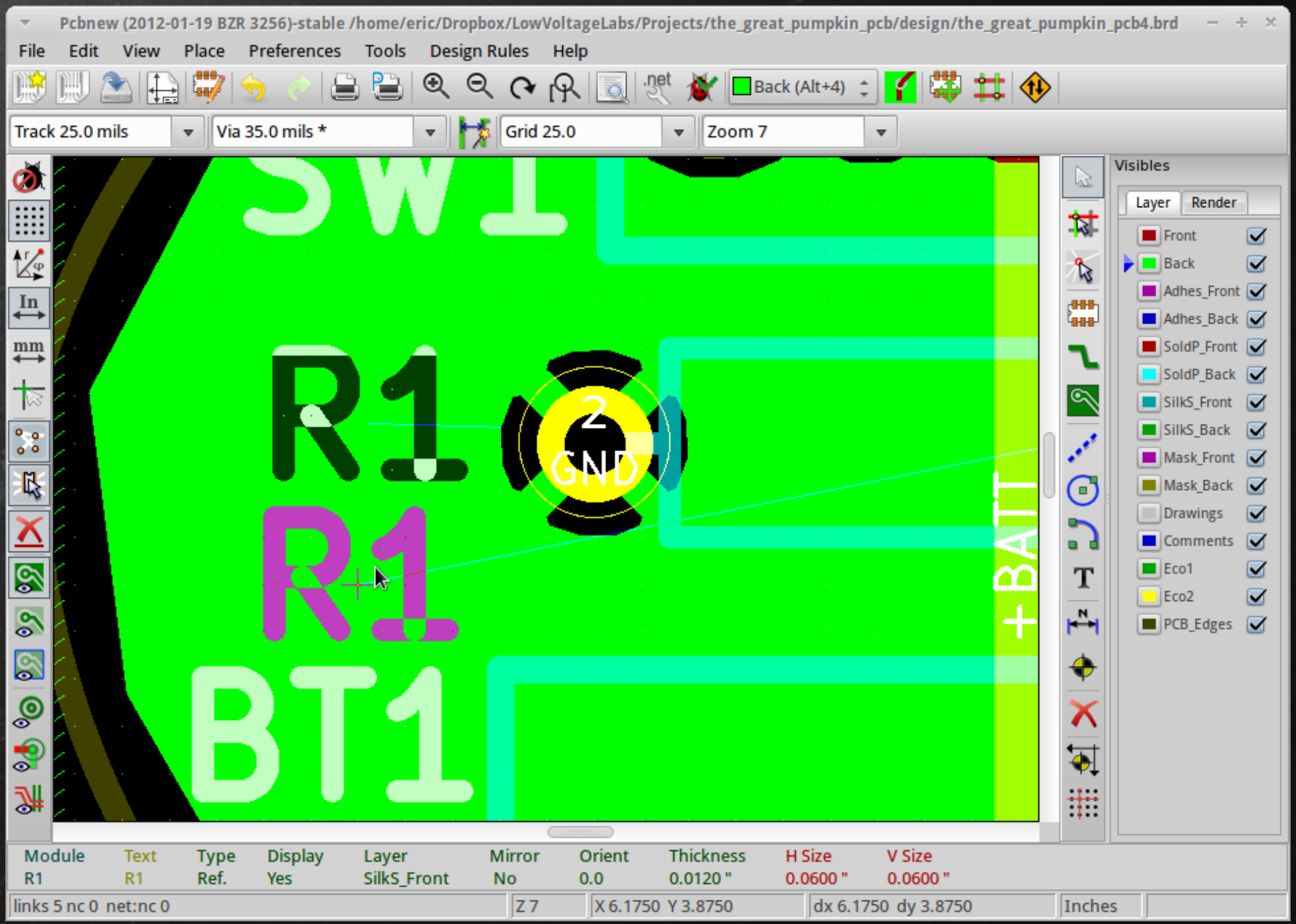

Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb4.brd
File
Edit
View
Place
Preferences
Tools
Design Rules
Help
Back (Alt+4)
Track 25.0 mils
Via 35.0 mils *
Grid 25.0
Auto
Visibles
Layer
Render
Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges
SW1
D1
R1
BT1
N-000004
N-000001
+BATT
GND
Pads
Vias
trackSegm
Nodes
Nets
Links
Connect
Unconnected
12
0
11
9
5
5
5
0
links 5 nc 0 net:nc 0
Z 22.5...
X 6.6250 Y 4.2750
dx 6.6250 dy 4.2750
Inches

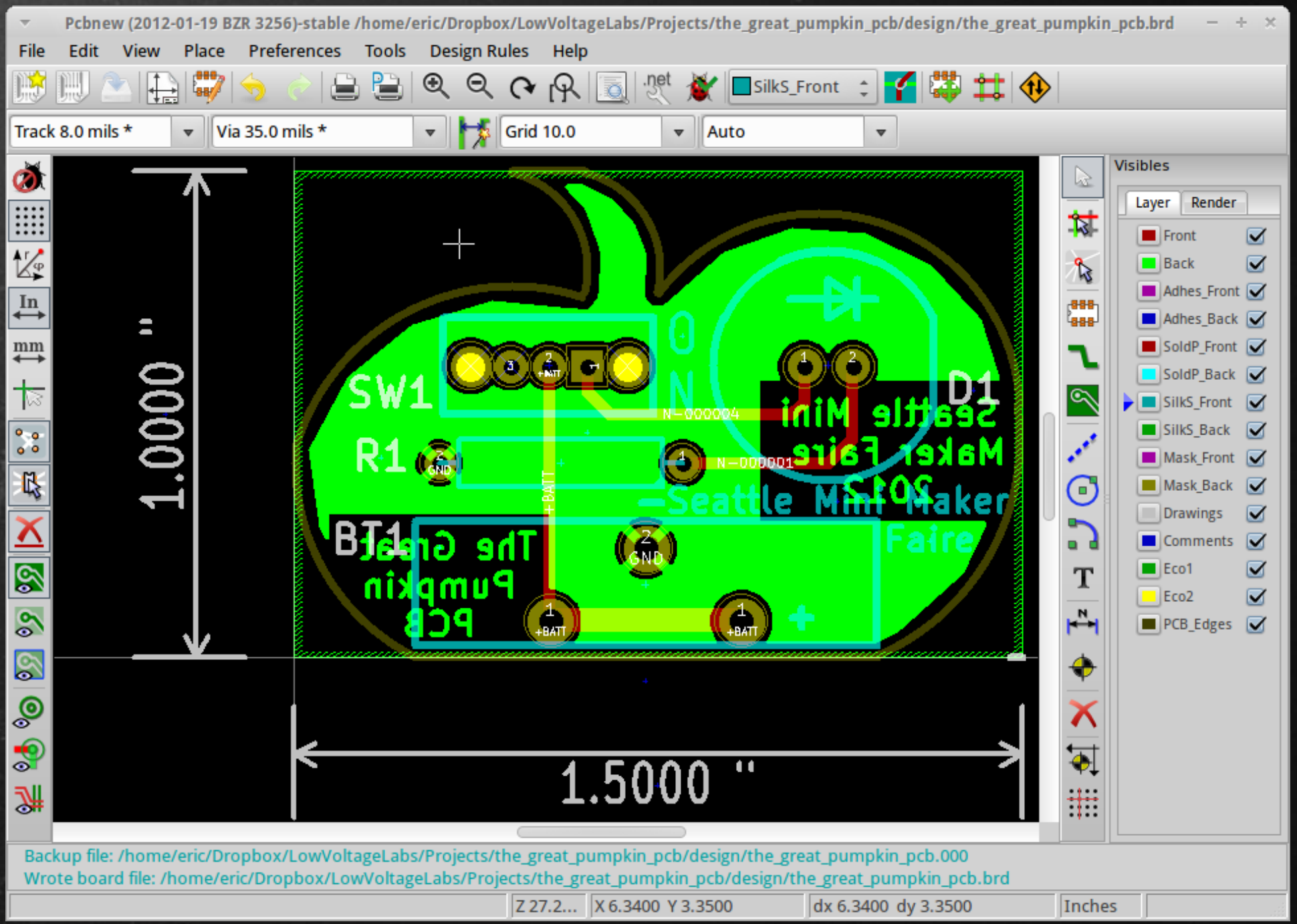
Place text on the board

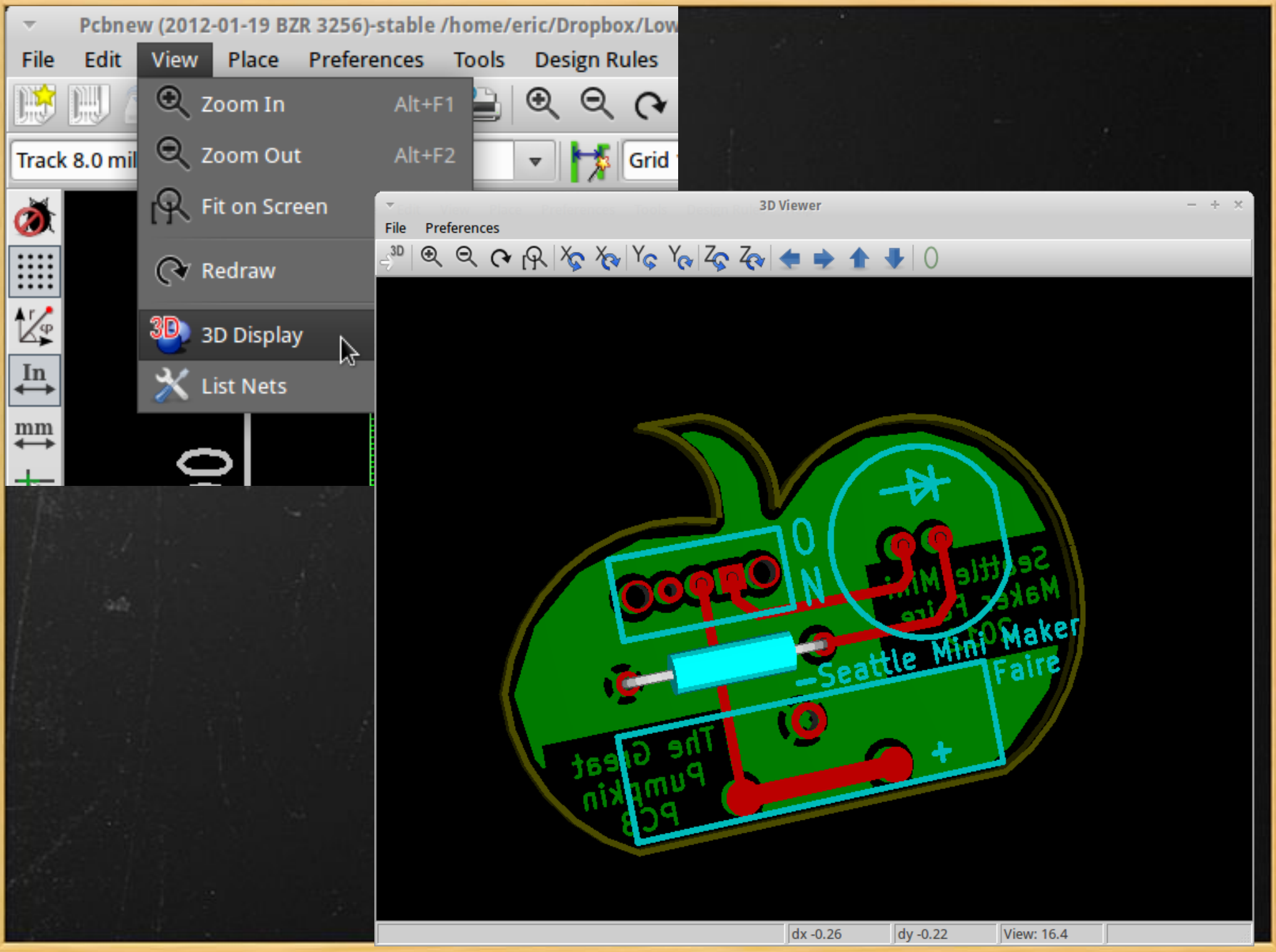


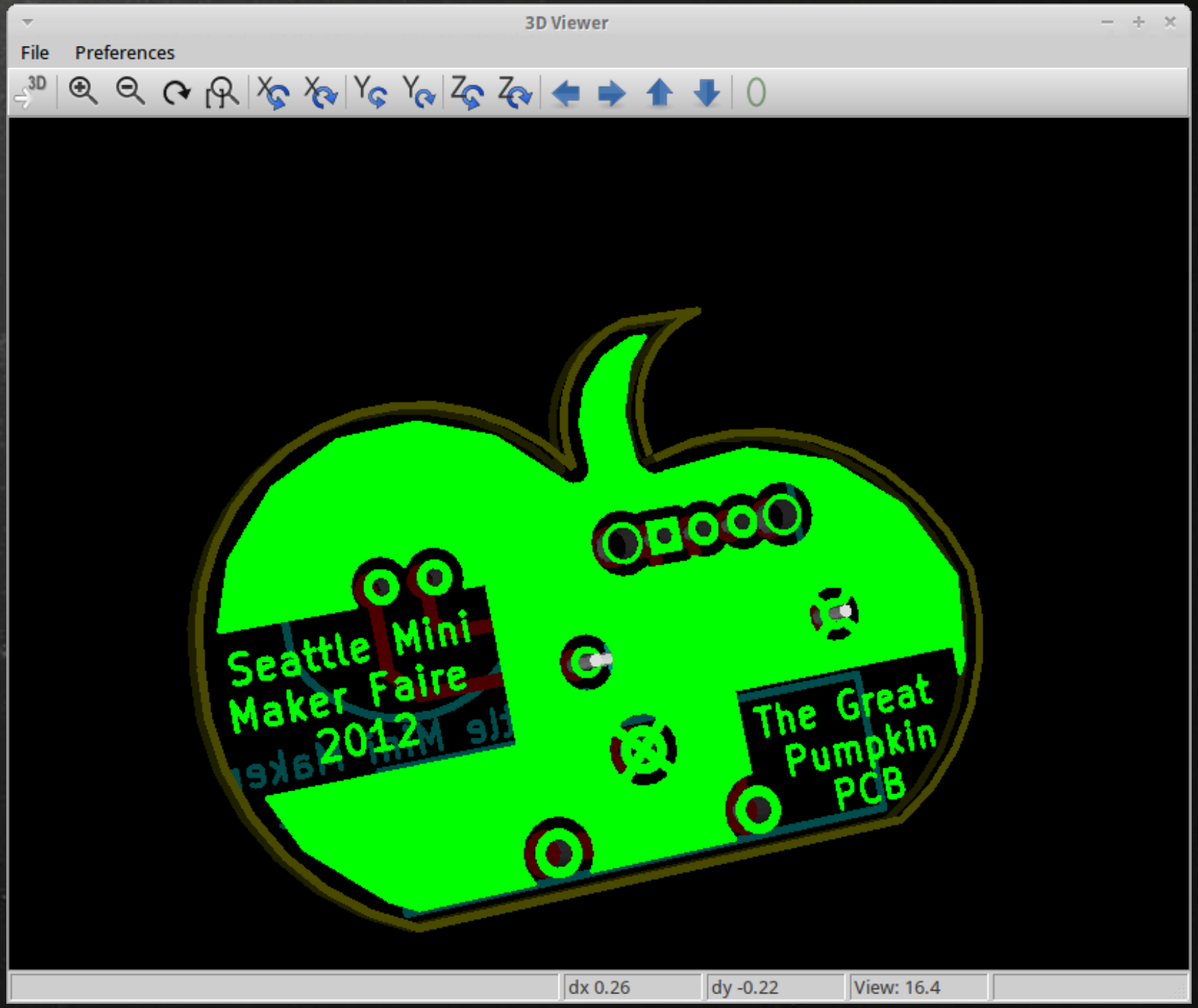
Back copper layer




Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb4.brd
File
Edit
View
Place
Preferences
Tools
Design Rules
Help
Back (Alt+4)
Track 25.0 mils
Via 35.0 mils *
Grid 25.0
Zoom 7
SW1
R1
2
GND
R1
BT1
+BATT
Visibles
Layer
Render
Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges
Module Text Type Display Layer Mirror Orient Thickness H Size V Size
R1 R1 Ref. Yes SilkS_Front No 0.0 0.0120 " 0.0600 " 0.0600 "
links 5 nc 0 net:nc 0
Z 7
X 6.1750 Y 3.8750
dx 6.1750 dy 3.8750
Inches

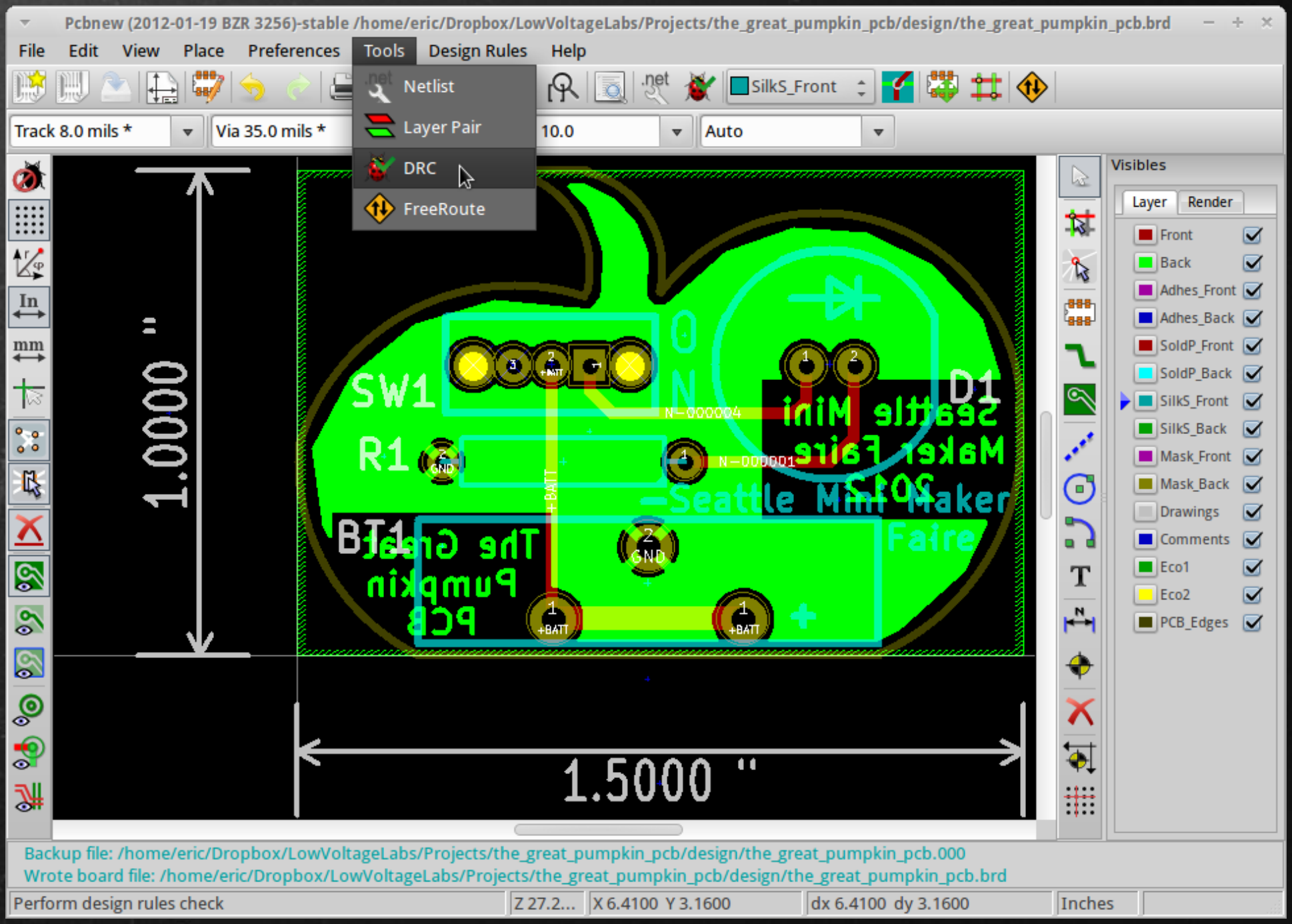

Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.brd
File Edit View Place Preferences Tools Design Rules Help
SilkS_Front
Track 8.0 mils *
Via 35.0 mils *
Grid 10.0
Auto
Visibles
Layer Render
Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges
SW1
R1
D1
BT1
ON
+BATT
GND
N-000004
N-000001
Seattle Mini Maker Faire
1.0000 "
1.5000 "
Backup file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.000
Wrote board file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.brd
Z 27.2...
X 6.3400 Y 3.3500
dx 6.3400 dy 3.3500
Inches


Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/Low
File
Edit
View
Place
Preferences
Tools
Design Rules
Zoom In Alt+F1
Zoom Out Alt+F2
Fit on Screen
Redraw
3D Display
List Nets
Track 8.0 mil
Grid
3D Viewer
File
Preferences
Seattle Mini Maker Faire
The Great Pumpkin PCB
dx -0.26
dy -0.22
View: 16.4

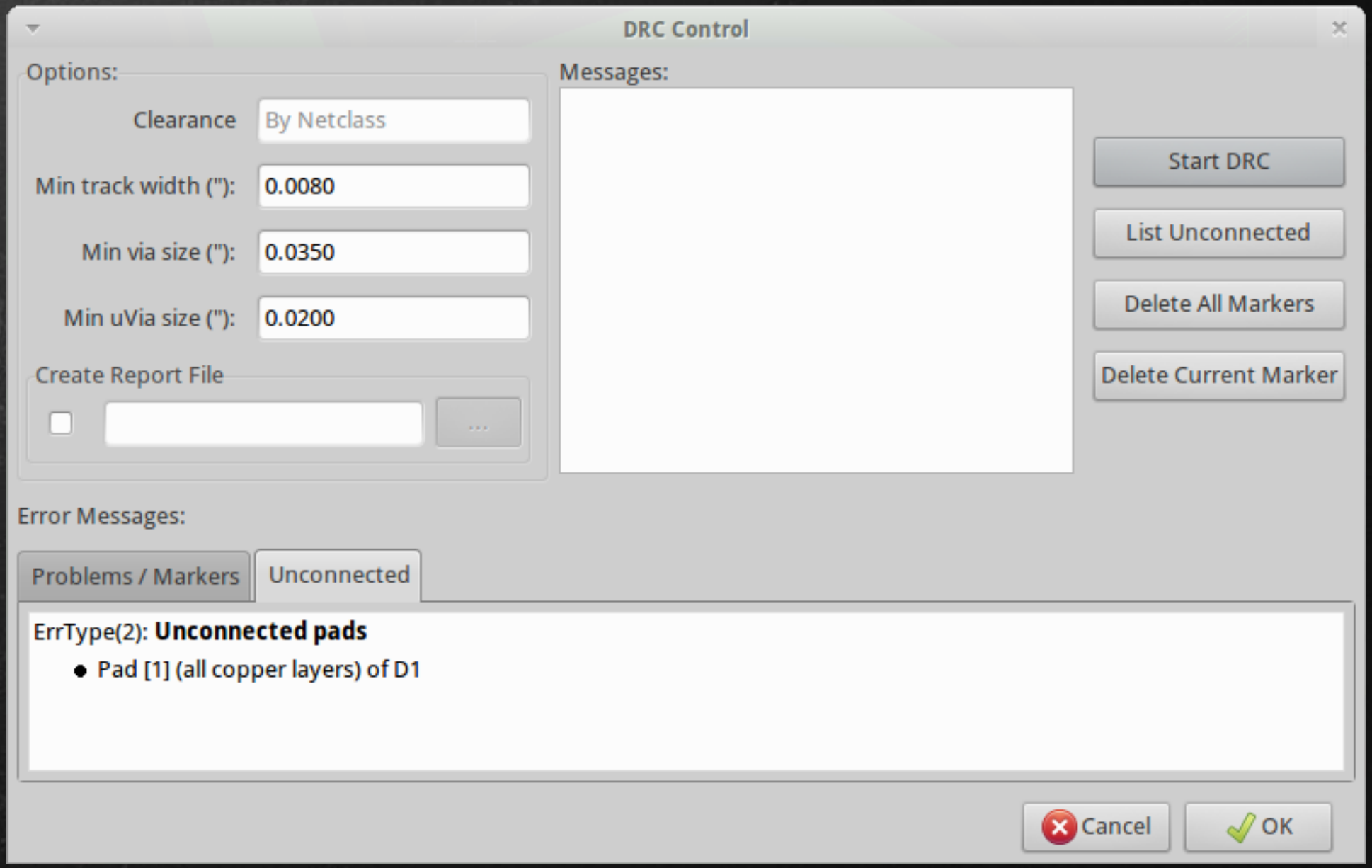

3D Viewer
File
Preferences
Seattle Mini
Maker Faire
2012
The Great
Pumpkin
PCB
dx 0.26
dy -0.22
View: 16.4

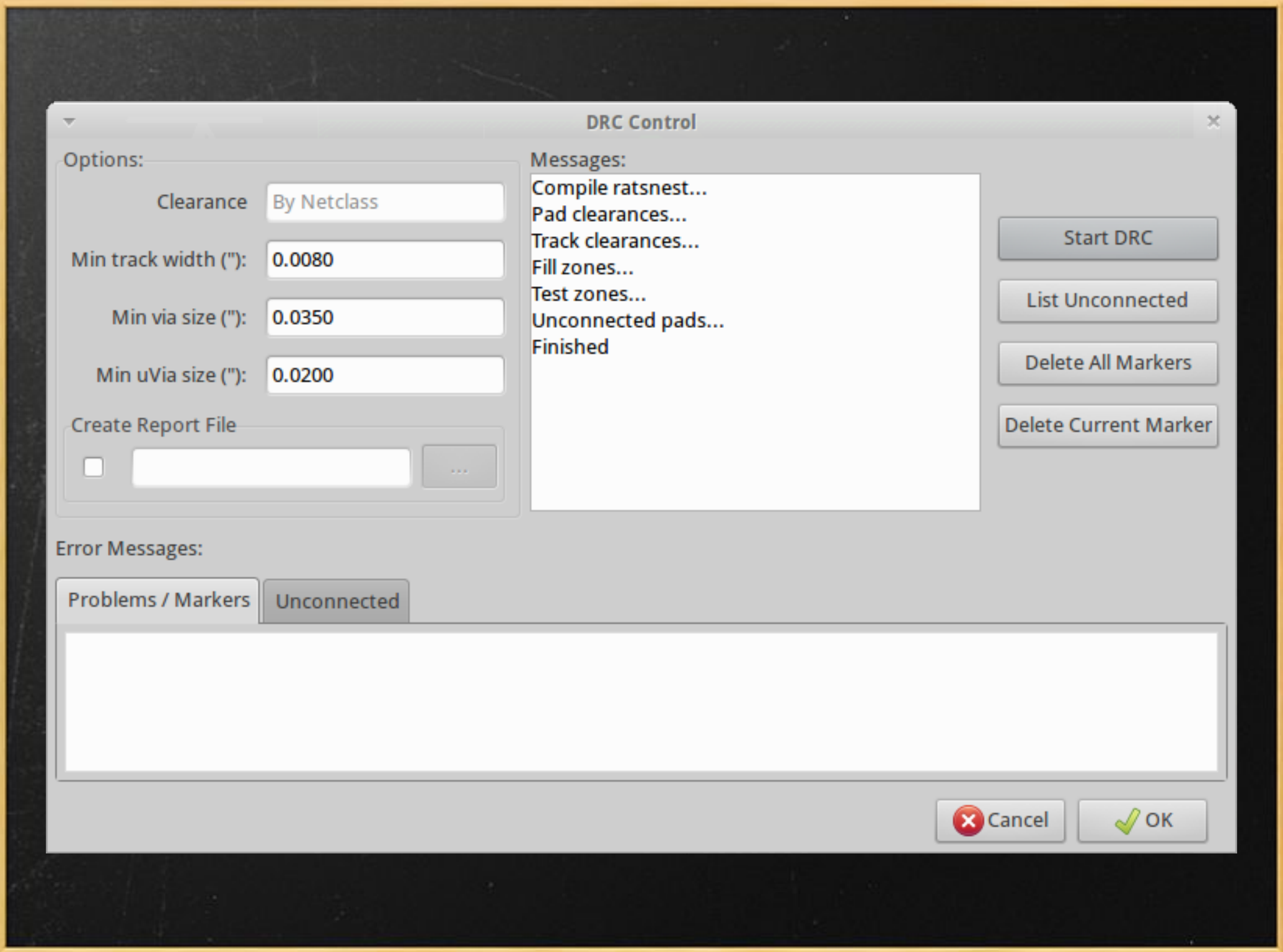
Create a board with KiCAD

- What is a PCB?
- What is a KiCAD?
- Block diagram
- Schematic
- Schematic attribute editor
- Error check the schematic
- PCB layout
- Error check the layout
- Gerber files
- Build boards


Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.brd
File
Edit
View
Place
Preferences
Tools
Design Rules
Help
Netlist
Layer Pair
DRC
FreeRoute
SilkS_Front
Track 8.0 mils *
Via 35.0 mils *
10.0
Auto
Visibles
Layer
Render
Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges
SW1
R1
D1
BT1
1.0000 "
1.5000 "
Backup file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.000
Wrote board file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.brd
Perform design rules check
Z 27.2...
X 6.4100 Y 3.1600
dx 6.4100 dy 3.1600
Inches

Check for unconnected pads




DRC Control
Options:
Clearance
By Netclass
Min track width (''):
0.0080
Min via size (''):
0.0350
Min uVia size (''):
0.0200
Create Report File
...
Messages:
Compile ratsnest...
Pad clearances...
Track clearances...
Fill zones...
Test zones...
Unconnected pads...
Finished
Start DRC
List Unconnected
Delete All Markers
Delete Current Marker
Error Messages:
Problems / Markers
Unconnected
Cancel
OK

Create a board with KiCAD

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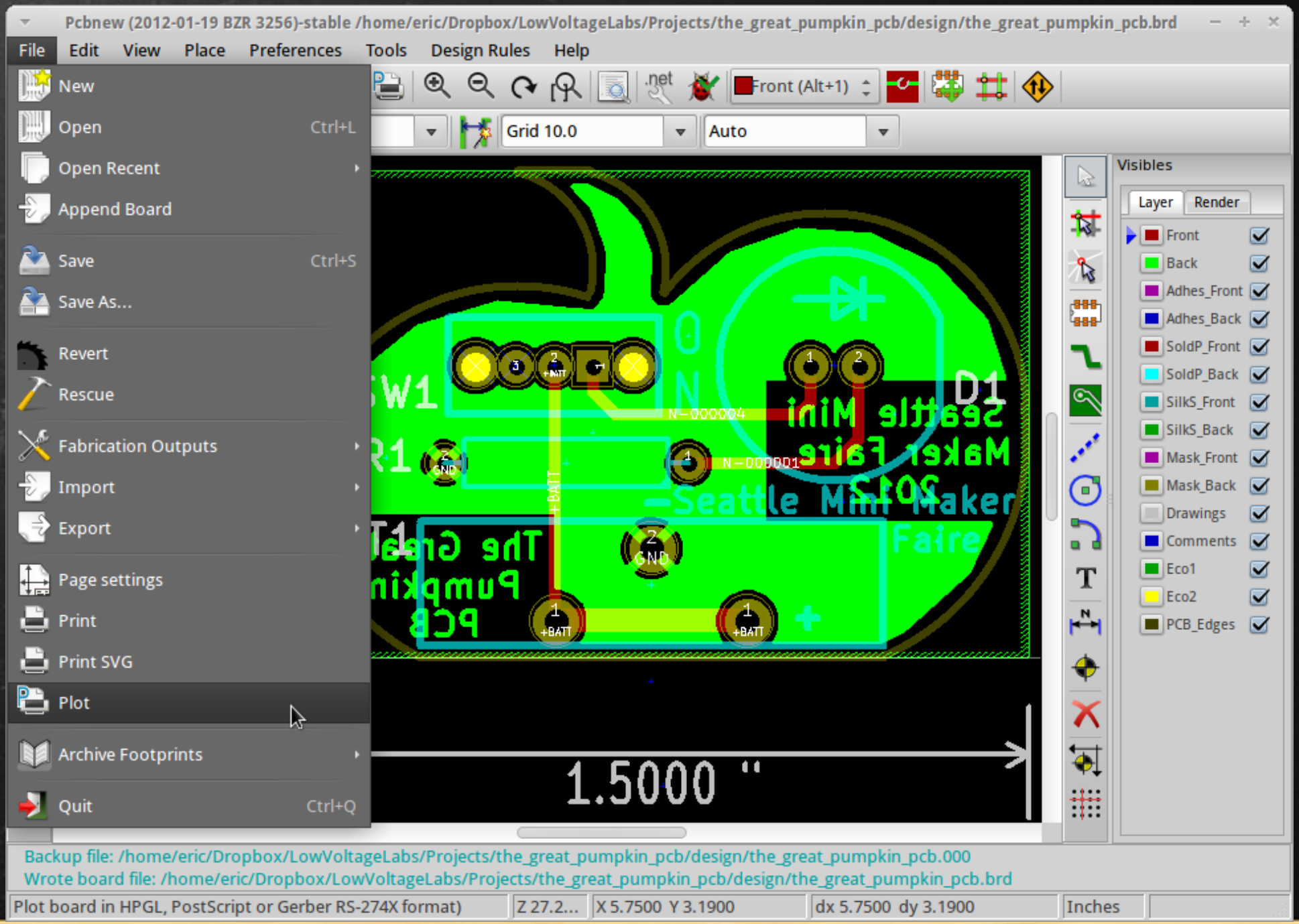
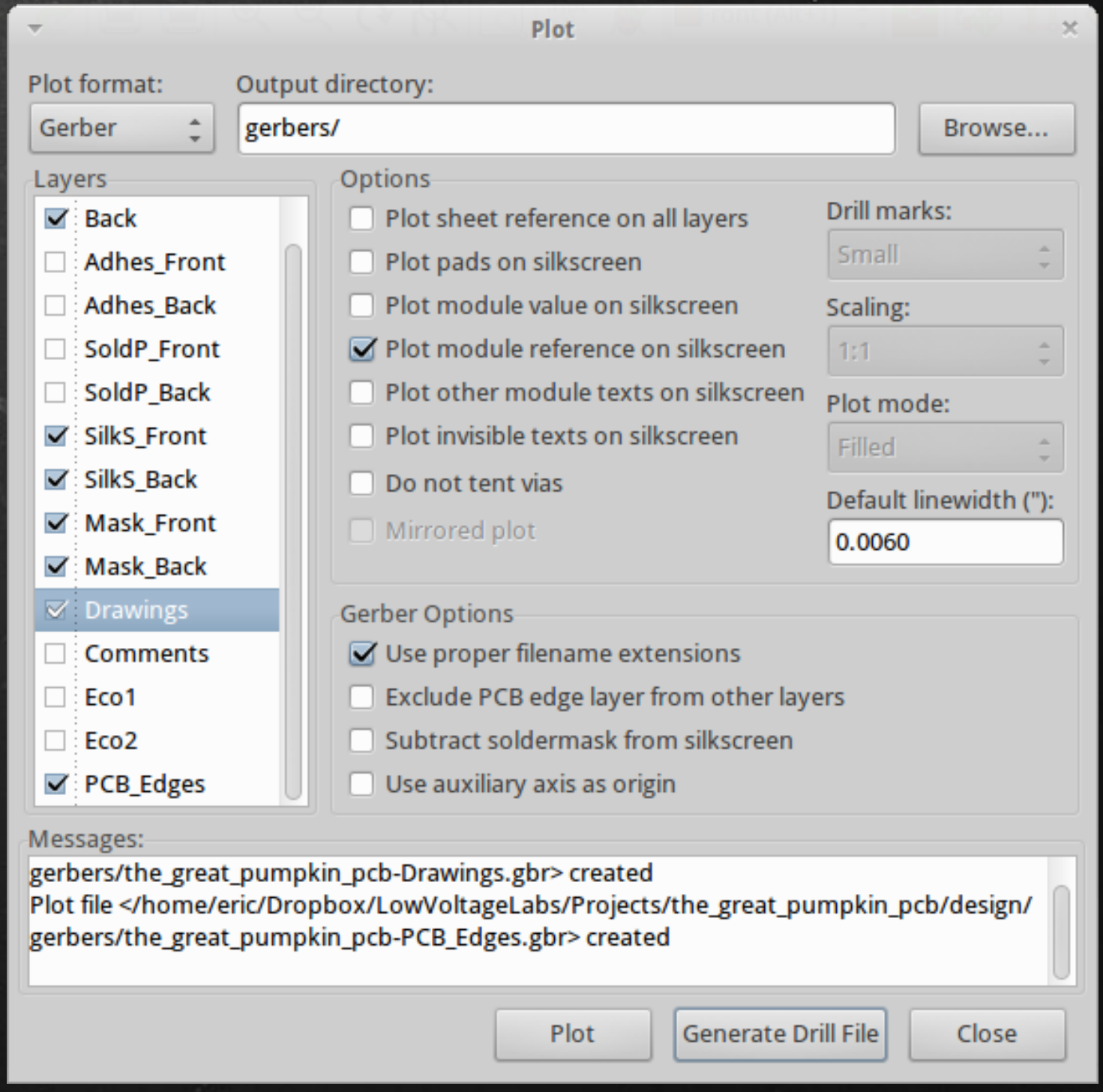
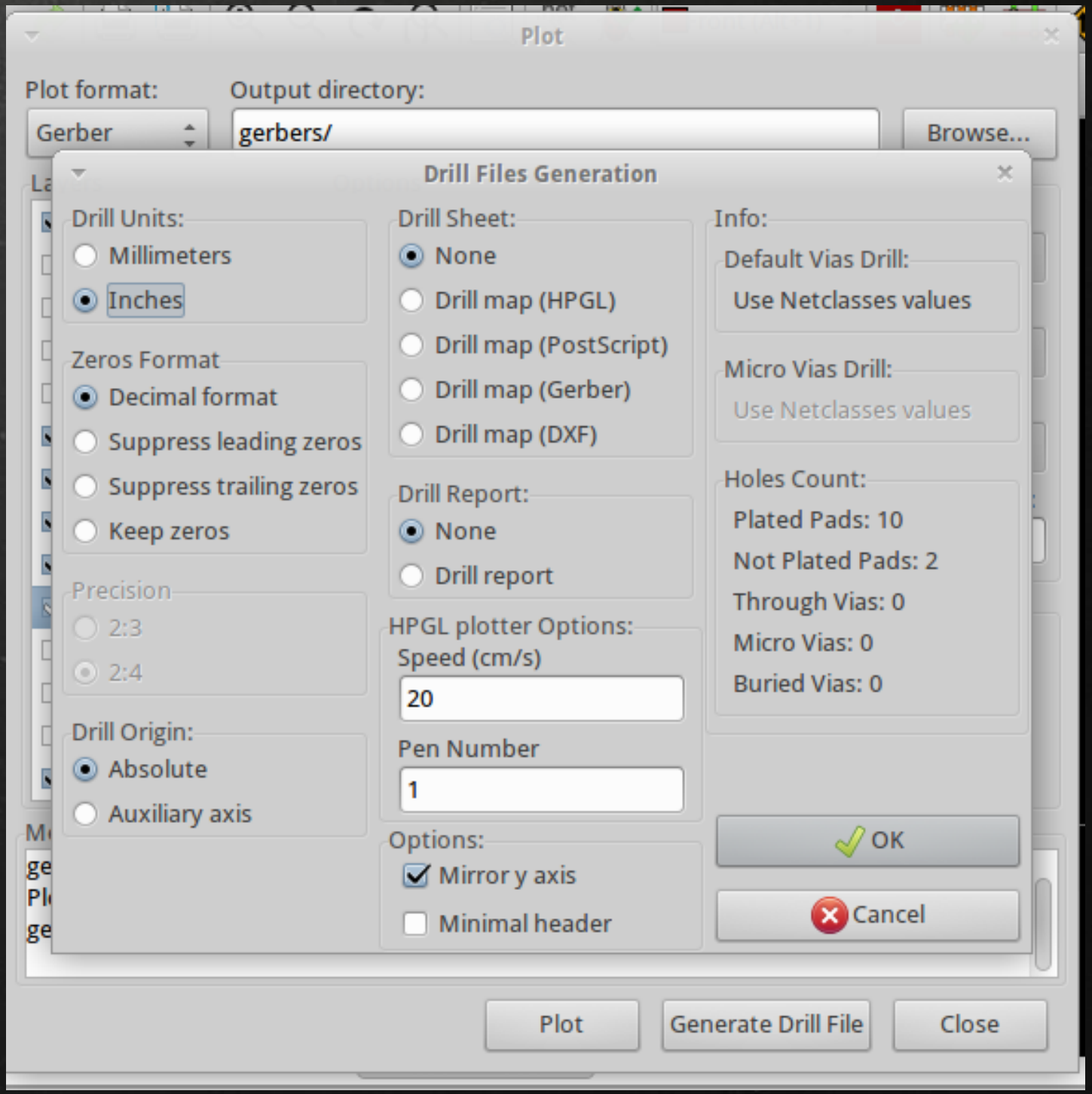
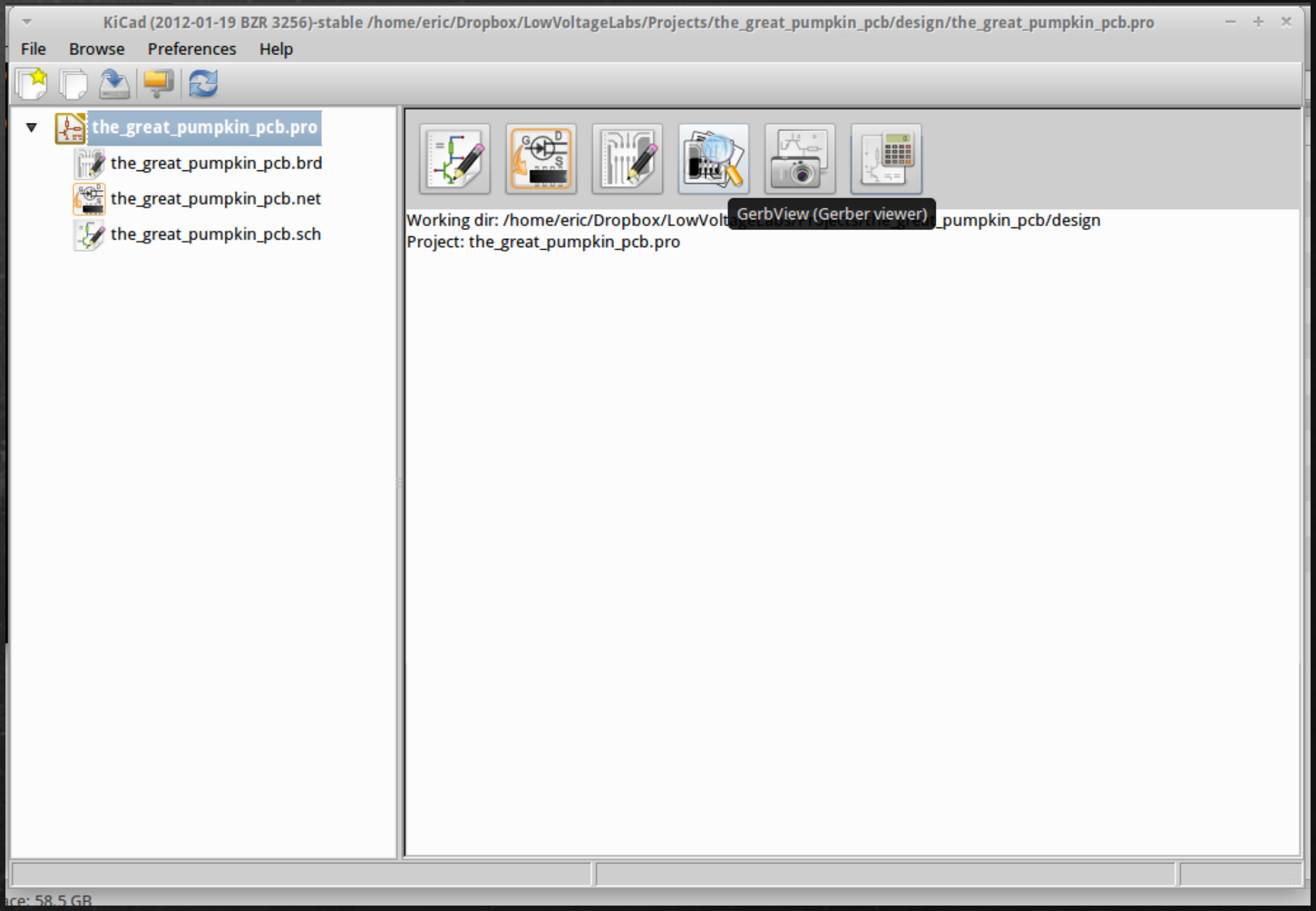
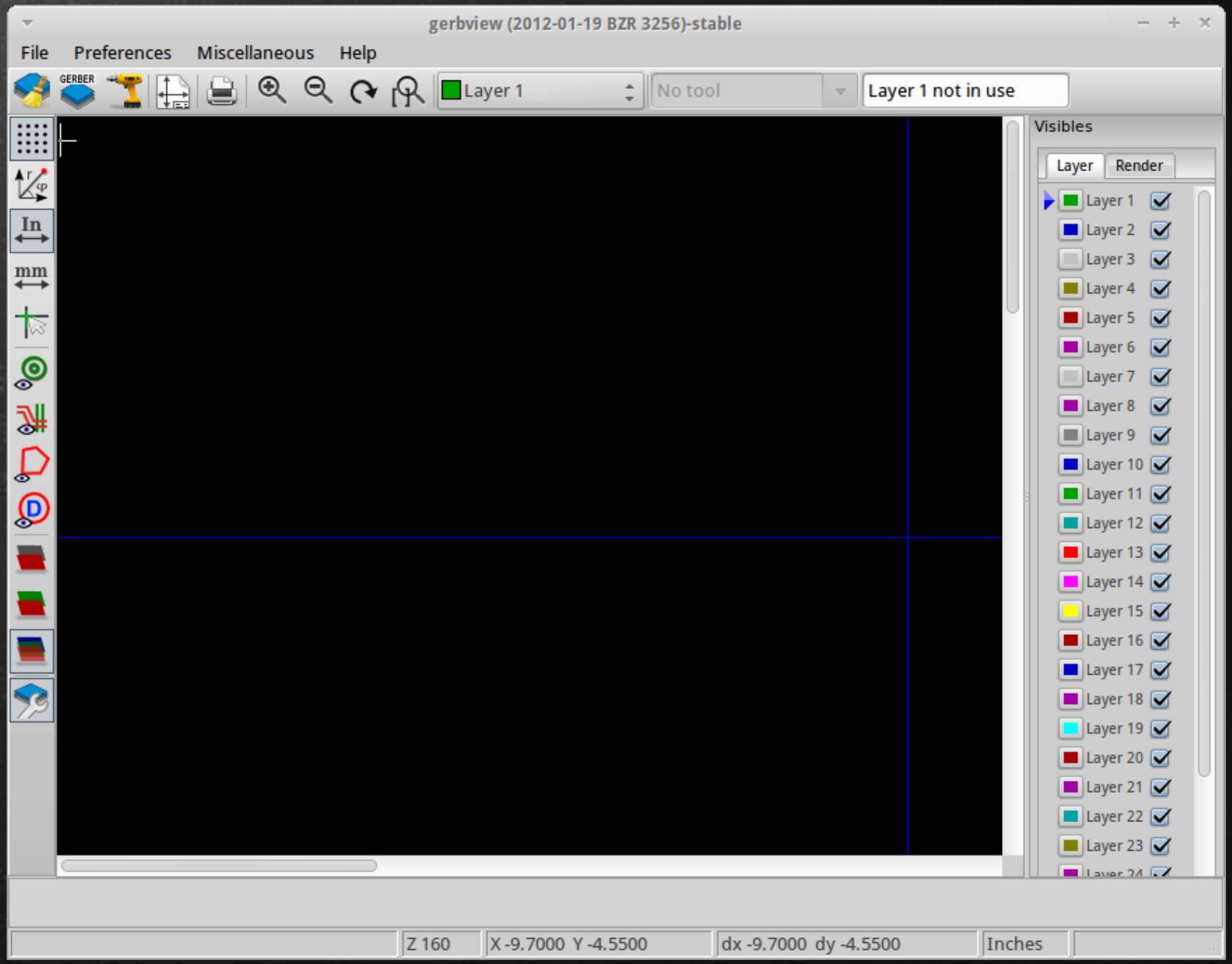
File -> Plot to generate gerber files

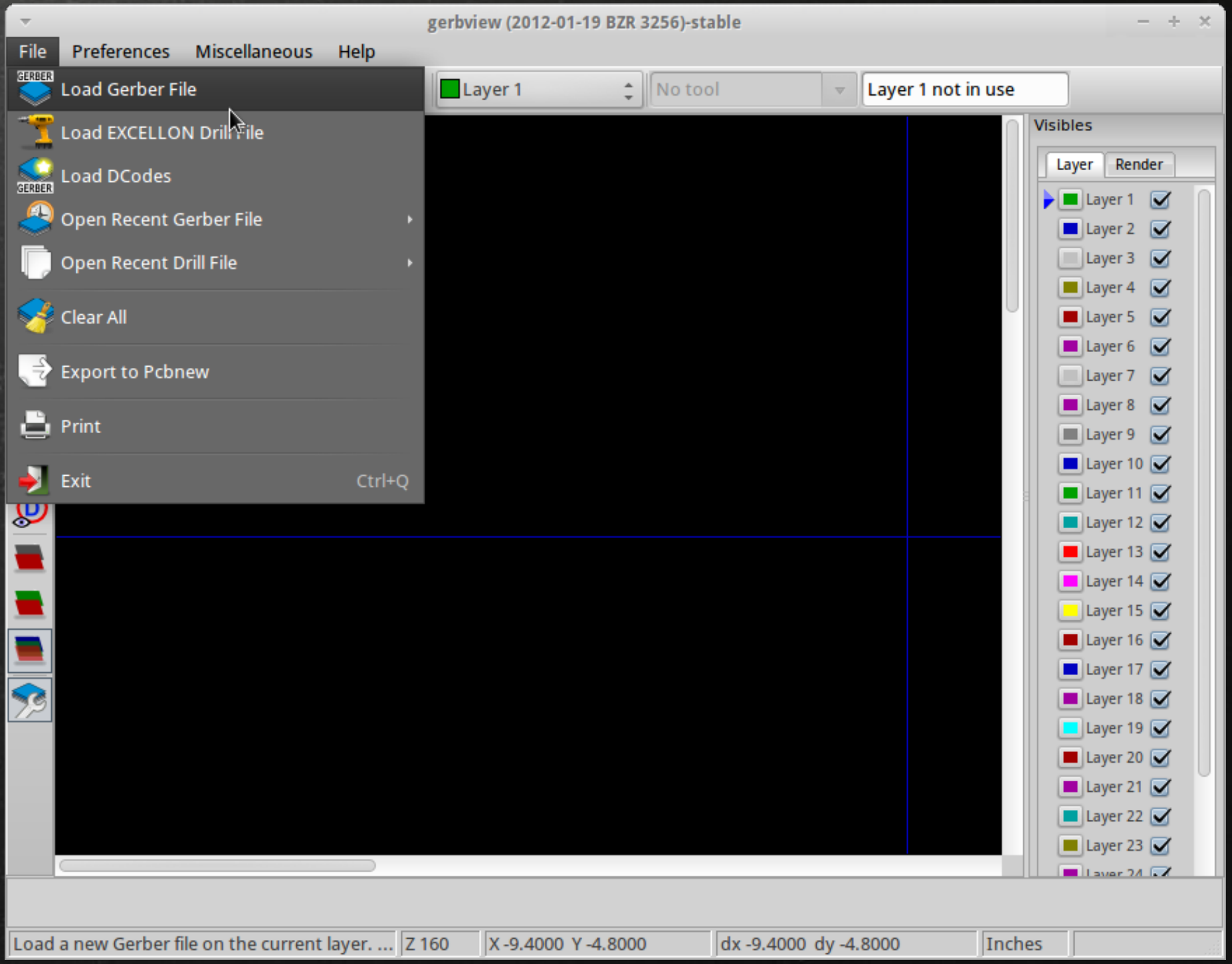


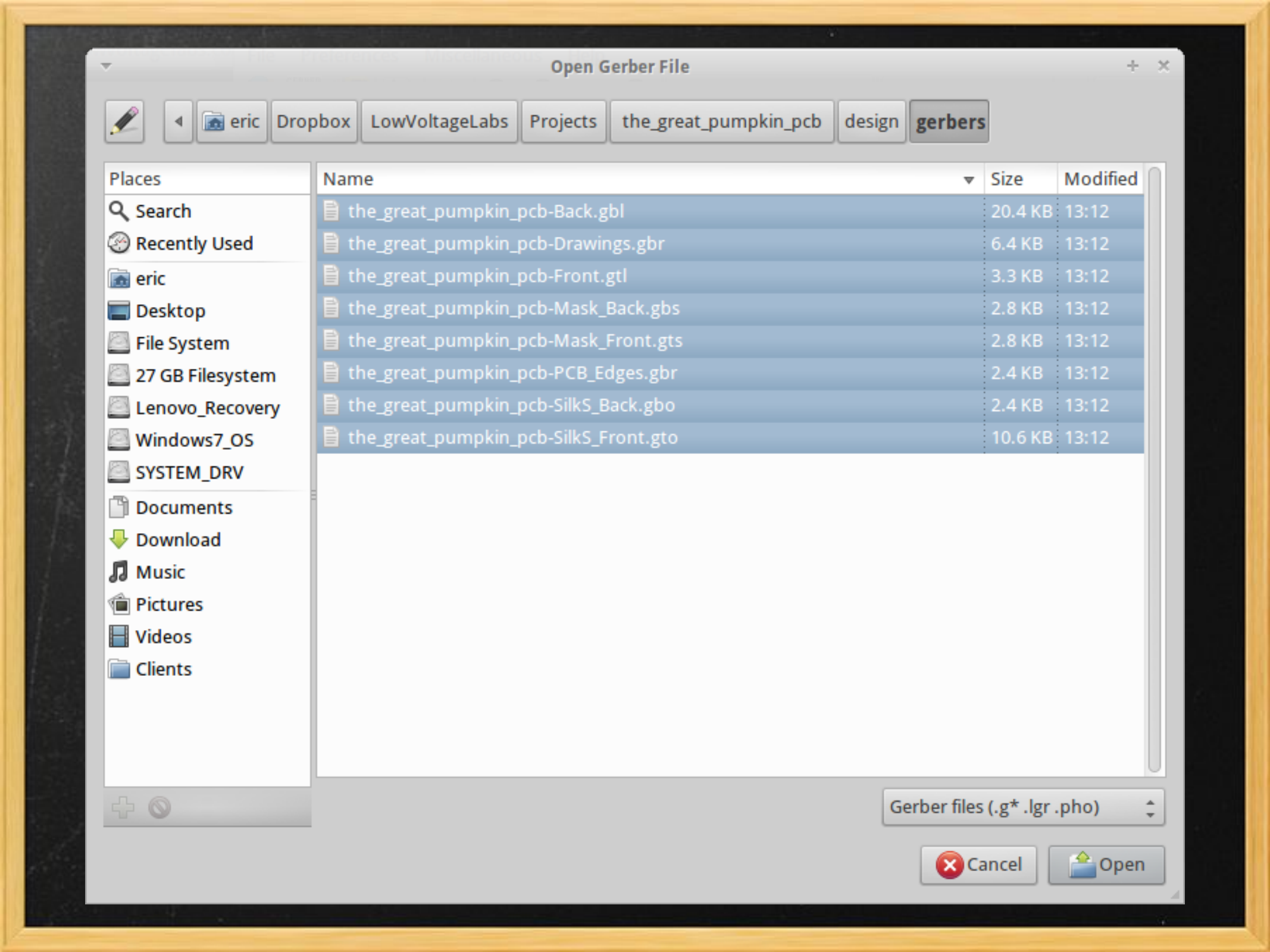

Plot
Plot format:
Gerber
Output directory:
gerbers/
Browse...
Layers
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges
Options
Plot sheet reference on all layers
Plot pads on silkscreen
Plot module value on silkscreen
Plot module reference on silkscreen
Plot other module texts on silkscreen
Plot invisible texts on silkscreen
Do not tent vias
Mirrored plot
Drill marks:
Small
Scaling:
1:1
Plot mode:
Filled
Default linewidth ("):
0.0060
Gerber Options
Use proper filename extensions
Exclude PCB edge layer from other layers
Subtract soldermask from silkscreen
Use auxiliary axis as origin
Messages:
gerbers/the_great_pumpkin_pcb-Drawings.gbr> created
Plot file </home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/
gerbers/the_great_pumpkin_pcb-PCB_Edges.gbr> created
Plot
Generate Drill File
Close

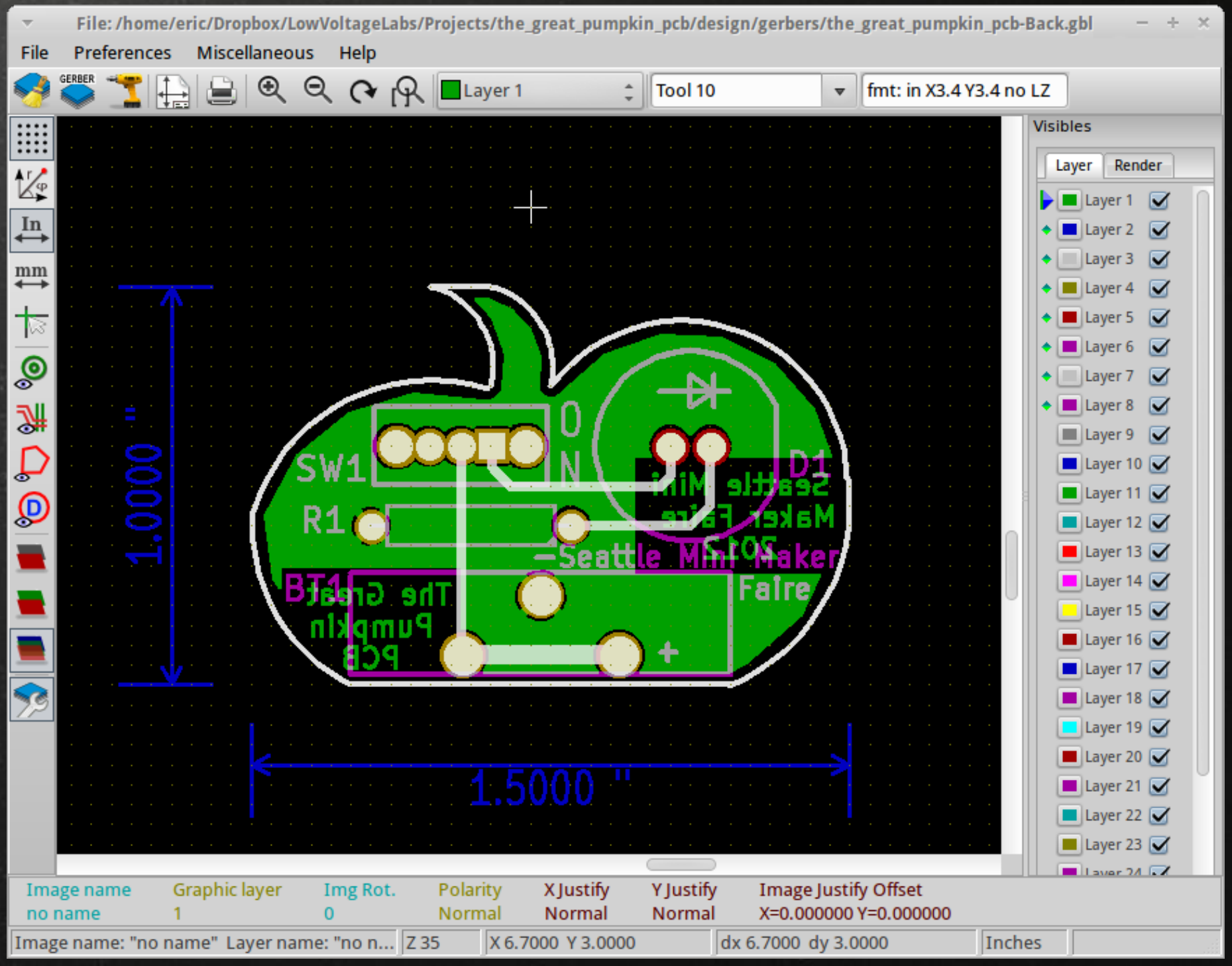

Plot
Plot format:
Gerber
Output directory:
gerbers/
Browse...
Drill Files Generation
Drill Units:
Millimeters
Inches
Zeros Format
Decimal format
Suppress leading zeros
Suppress trailing zeros
Keep zeros
Precision
2:3
2:4
Drill Origin:
Absolute
Auxiliary axis
Drill Sheet:
None
Drill map (HPGL)
Drill map (PostScript)
Drill map (Gerber)
Drill map (DXF)
Drill Report:
None
Drill report
HPGL plotter Options:
Speed (cm/s)
20
Pen Number
1
Options:
Mirror y axis
Minimal header
Info:
Default Vias Drill:
Use Netclasses values
Micro Vias Drill:
Use Netclasses values
Holes Count:
Plated Pads: 10
Not Plated Pads: 2
Through Vias: 0
Micro Vias: 0
Buried Vias: 0
OK
Cancel
Plot
Generate Drill File
Close

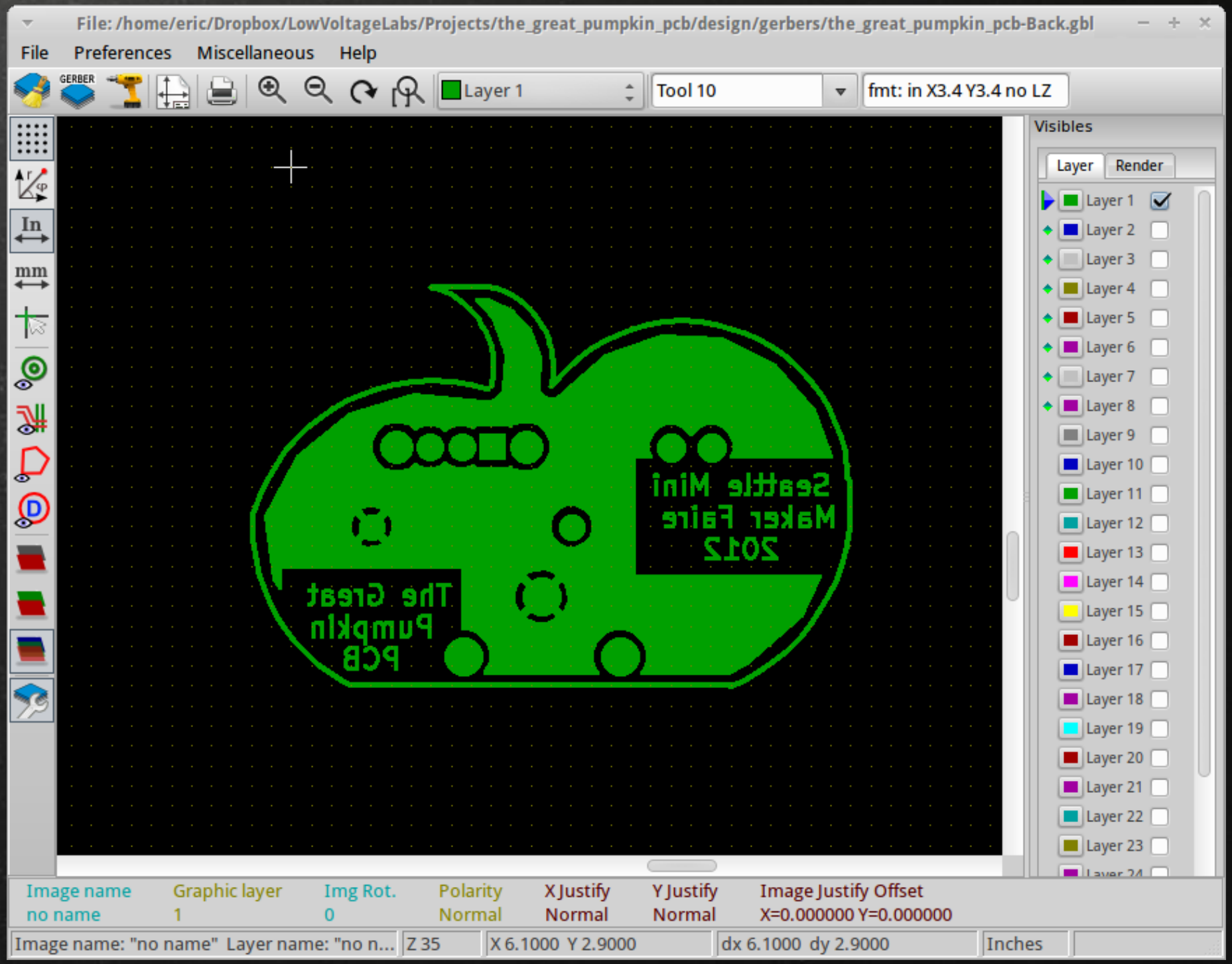

KiCad (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.pro
File
Browse
Preferences
Help
the_great_pumpkin_pcb.pro
the_great_pumpkin_pcb.brd
the_great_pumpkin_pcb.net
the_great_pumpkin_pcb.sch
GerbView (Gerber viewer)
Working dir: /home/eric/Dropbox/LowVolt
_pumpkin_pcb/design
Project: the_great_pumpkin_pcb.pro

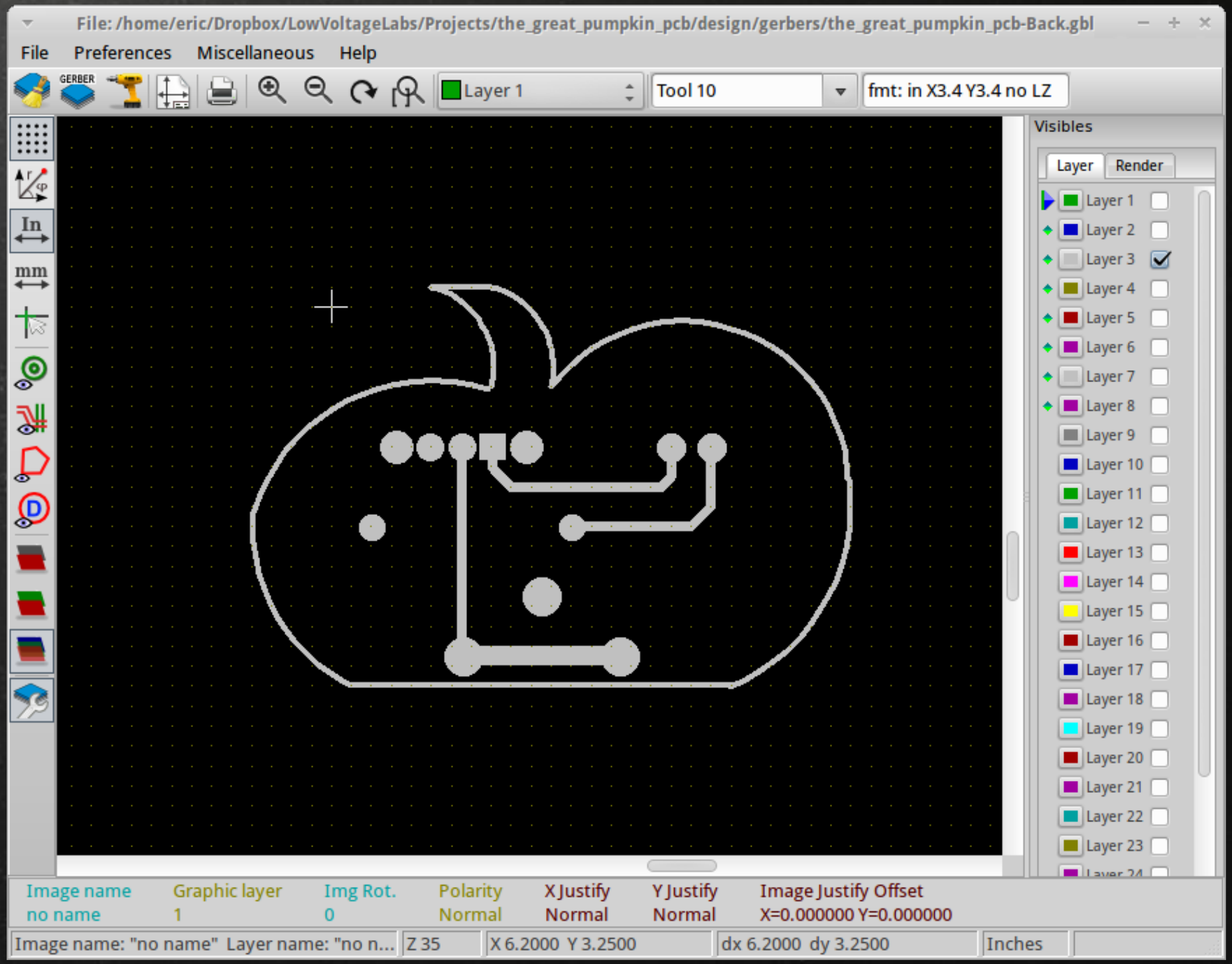

gerbview (2012-01-19 BZR 3256)-stable
File
Preferences
Miscellaneous
Help
GERBER
Layer 1
No tool
Layer 1 not in use
In
mm
Visibles
Layer
Render
Layer 1
Layer 2
Layer 3
Layer 4
Layer 5
Layer 6
Layer 7
Layer 8
Layer 9
Layer 10
Layer 11
Layer 12
Layer 13
Layer 14
Layer 15
Layer 16
Layer 17
Layer 18
Layer 19
Layer 20
Layer 21
Layer 22
Layer 23
Z 160
X -9.7000 Y -4.5500
dx -9.7000 dy -4.5500
Inches

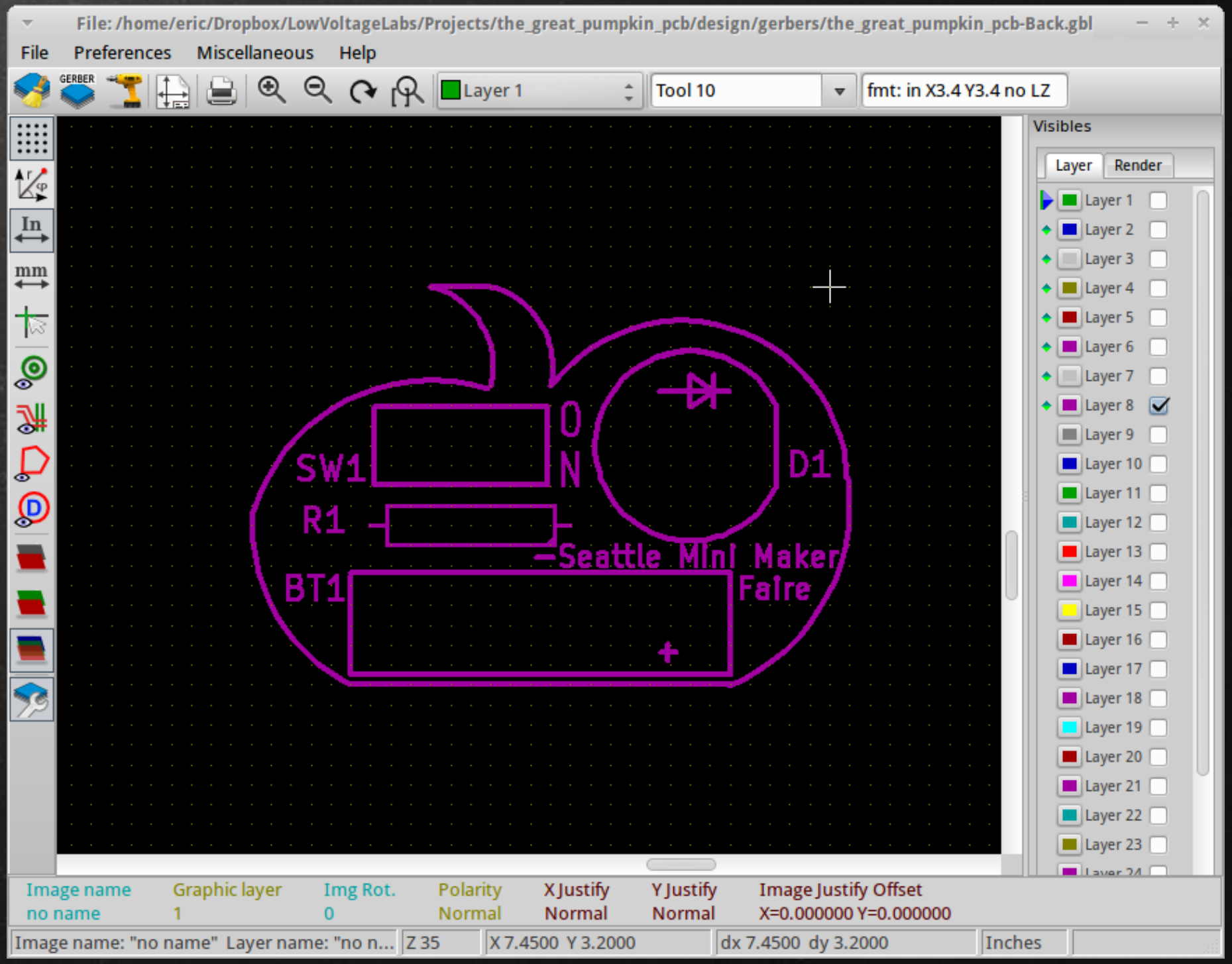

gerbview (2012-01-19 BZR 3256)-stable
File
Preferences
Miscellaneous
Help
Load Gerber File
Load EXCELLON Drill File
Load DCodes
Open Recent Gerber File
Open Recent Drill File
Clear All
Export to Pcbnew
Print
Exit
Ctrl+Q
Layer 1
No tool
Layer 1 not in use
Visibles
Layer
Render
Layer 1
Layer 2
Layer 3
Layer 4
Layer 5
Layer 6
Layer 7
Layer 8
Layer 9
Layer 10
Layer 11
Layer 12
Layer 13
Layer 14
Layer 15
Layer 16
Layer 17
Layer 18
Layer 19
Layer 20
Layer 21
Layer 22
Layer 23
Load a new Gerber file on the current layer. ...
Z 160
X -9.4000 Y -4.8000
dx -9.4000 dy -4.8000
Inches

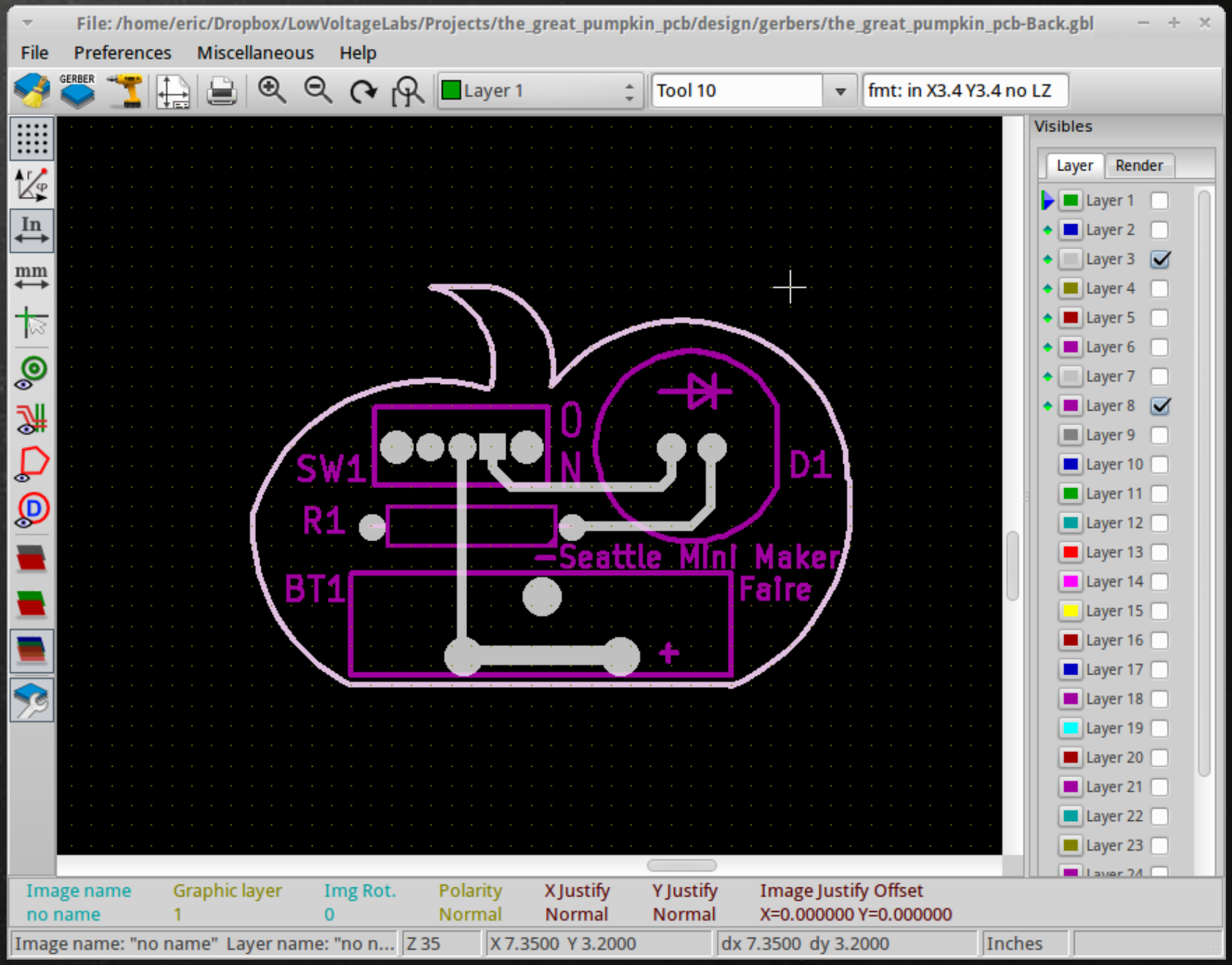

Open Gerber File
eric
Dropbox
LowVoltageLabs
Projects
the_great_pumpkin_pcb
design
gerbers
Places
Search
Recently Used
eric
Desktop
File System
27 GB Filesystem
Lenovo_Recovery
Windows7_OS
SYSTEM_DRV
Documents
Download
Music
Pictures
Videos
Clients
Name
Size
Modified
the_great_pumpkin_pcb-Back.gbl 20.4 KB 13:12
the_great_pumpkin_pcb-Drawings.gbr 6.4 KB 13:12
the_great_pumpkin_pcb-Front.gtl 3.3 KB 13:12
the_great_pumpkin_pcb-Mask_Back.gbs 2.8 KB 13:12
the_great_pumpkin_pcb-Mask_Front.gts 2.8 KB 13:12
the_great_pumpkin_pcb-PCB_Edges.gbr 2.4 KB 13:12
the_great_pumpkin_pcb-SilkS_Back.gbo 2.4 KB 13:12
the_great_pumpkin_pcb-SilkS_Front.gto 10.6 KB 13:12
Gerber files (.g* .lgr .pho)
Cancel
Open


File: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/gerbers/the_great_pumpkin_pcb-Back.gbl
File
Preferences
Miscellaneous
Help
GERBER
Layer 1
Tool 10
fmt: in X3.4 Y3.4 no LZ
Visibles
Layer
Render
Layer 1
Layer 2
Layer 3
Layer 4
Layer 5
Layer 6
Layer 7
Layer 8
Layer 9
Layer 10
Layer 11
Layer 12
Layer 13
Layer 14
Layer 15
Layer 16
Layer 17
Layer 18
Layer 19
Layer 20
Layer 21
Layer 22
Layer 23
SW1
R1
D1
BT1
1.0000 "
1.5000 "
Image name
no name
Graphic layer
1
Img Rot.
0
Polarity
Normal
X Justify
Normal
Y Justify
Normal
Image Justify Offset
X=0.000000 Y=0.000000
Image name: "no name" Layer name: "no n...
Z 35
X 6.7000 Y 3.0000
dx 6.7000 dy 3.0000
Inches


File: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/gerbers/the_great_pumpkin_pcb-Back.gbl
File
Preferences
Miscellaneous
Help
GERBER
Layer 1
Tool 10
fmt: in X3.4 Y3.4 no LZ
In
mm
Visibles
Layer
Render
Layer 1
Layer 2
Layer 3
Layer 4
Layer 5
Layer 6
Layer 7
Layer 8
Layer 9
Layer 10
Layer 11
Layer 12
Layer 13
Layer 14
Layer 15
Layer 16
Layer 17
Layer 18
Layer 19
Layer 20
Layer 21
Layer 22
Layer 23
Seattle Mini Maker Faire 2012
The Great Pumpkin PCB
Image name
no name
Graphic layer
1
Img Rot.
0
Polarity
Normal
X Justify
Normal
Y Justify
Normal
Image Justify Offset
X=0.000000 Y=0.000000
Image name: "no name" Layer name: "no n...
Z 35
X 6.1000 Y 2.9000
dx 6.1000 dy 2.9000
Inches


File: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/gerbers/the_great_pumpkin_pcb-Back.gbl
File
Preferences
Miscellaneous
Help
GERBER
Layer 1
Tool 10
fmt: in X3.4 Y3.4 no LZ
In
mm
Visibles
Layer
Render
Layer 1
Layer 2
Layer 3
Layer 4
Layer 5
Layer 6
Layer 7
Layer 8
Layer 9
Layer 10
Layer 11
Layer 12
Layer 13
Layer 14
Layer 15
Layer 16
Layer 17
Layer 18
Layer 19
Layer 20
Layer 21
Layer 22
Layer 23
Image name
no name
Graphic layer
1
Img Rot.
0
Polarity
Normal
X Justify
Normal
Y Justify
Normal
Image Justify Offset
X=0.000000 Y=0.000000
Image name: "no name" Layer name: "no n...
Z 35
X 6.2000 Y 3.2500
dx 6.2000 dy 3.2500
Inches


File: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/gerbers/the_great_pumpkin_pcb-Back.gbl
File
Preferences
Miscellaneous
Help
GERBER
Layer 1
Tool 10
fmt: in X3.4 Y3.4 no LZ
Visibles
Layer
Render
Layer 1
Layer 2
Layer 3
Layer 4
Layer 5
Layer 6
Layer 7
Layer 8
Layer 9
Layer 10
Layer 11
Layer 12
Layer 13
Layer 14
Layer 15
Layer 16
Layer 17
Layer 18
Layer 19
Layer 20
Layer 21
Layer 22
Layer 23
SW1
ON
D1
R1
Seattle Mini Maker Faire
BT1
+
Image name
no name
Graphic layer
1
Img Rot.
0
Polarity
Normal
X Justify
Normal
Y Justify
Normal
Image Justify Offset
X=0.000000 Y=0.000000
Image name: "no name" Layer name: "no n...
Z 35
X 7.4500 Y 3.2000
dx 7.4500 dy 3.2000
Inches


File: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/gerbers/the_great_pumpkin_pcb-Back.gbl
File
Preferences
Miscellaneous
Help
GERBER
Layer 1
Tool 10
fmt: in X3.4 Y3.4 no LZ
Visibles
Layer
Render
Layer 1
Layer 2
Layer 3
Layer 4
Layer 5
Layer 6
Layer 7
Layer 8
Layer 9
Layer 10
Layer 11
Layer 12
Layer 13
Layer 14
Layer 15
Layer 16
Layer 17
Layer 18
Layer 19
Layer 20
Layer 21
Layer 22
Layer 23
SW1
ON
D1
R1
BT1
Seattle Mini Maker Faire
+
Image name
no name
Graphic layer
1
Img Rot.
0
Polarity
Normal
X Justify
Normal
Y Justify
Normal
Image Justify Offset
X=0.000000 Y=0.000000
Image name: "no name" Layer name: "no n...
Z 35
X 7.3500 Y 3.2000
dx 7.3500 dy 3.2000
Inches

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PCB price factors:

- complexity - small space/trace or special features
- size of the board and number of boards
- turn around time

PCB Pooling Services

DorkbotPDX PCB http://dorkbotpdx.org/wiki/pcb_order

- Qty=3, two-layer boards: $5 per square inch
- Today's board example would be ~$7.50 for qty=3
- Qty=3, four-layer boards: $10 per square inch
- Purple solder mask
- 2 layer boards ship approx in 14 days
- Prices include shipping

Midnight Maker http://www.midnightmaker.com/

- Qty=3, two-layer boards: $5 per square inch
- Today's board example would be ~$7.50 for qty=3
- Qty=3, four-layer boards: $10 per square inch
- Black solder mask
- One week manufacturing time
- Prices include shipping

PCB Service Companies

Sunstone http://www.sunstone.com/

- Mulino, OR
- ValueProto service
- Today's example board would cost $38.50, qty=3
- Available in two weeks or less includes shipping
- Also have more options for faster turn around time

Seeed Studio
http://www.seeedstudio.com/

- Fusion PCB service
- $9.90 for 10 boards up to 5cm X 5cm in size
- Today's example board would cost $9.90, Qty=10
- Plus shipping $4.10 to ship to the State of Washington
- Shipping 10-30 to the US

PCB samples thanks to:
DorkbotPDX PCB
Midnight Maker
Seeed Studio

Eric Thompson
LowVoltageLabs.com