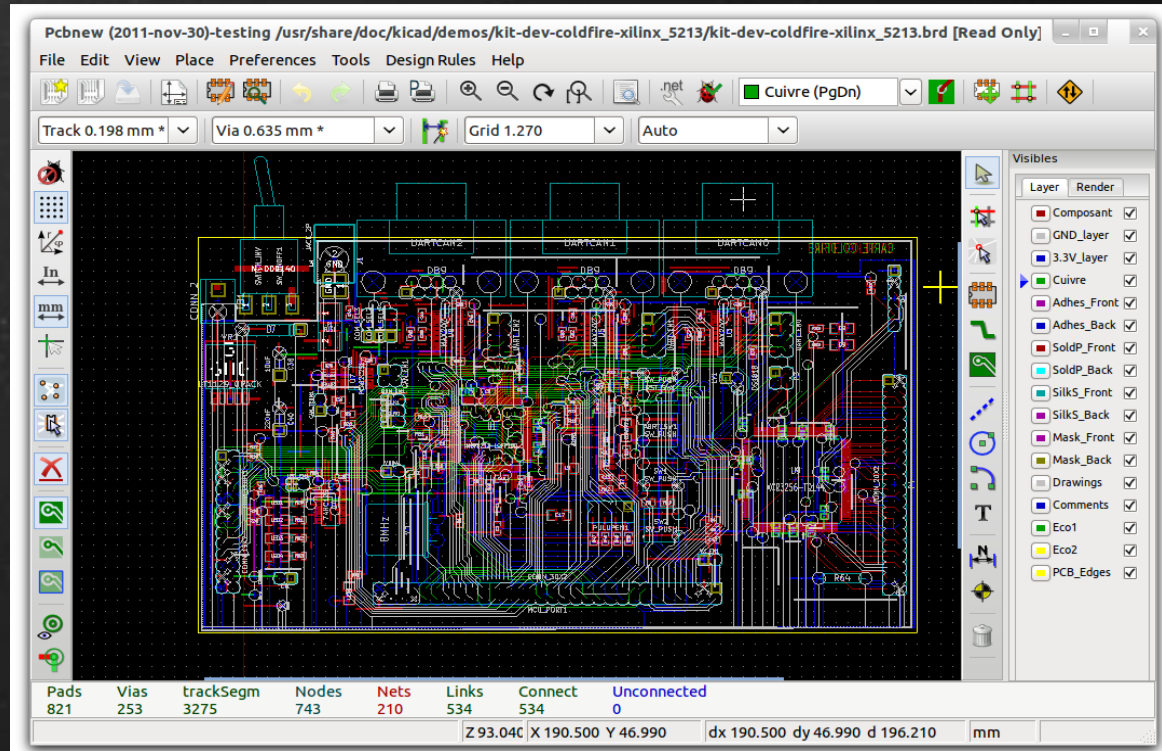


Release your hardware hacker potential with KiCAD

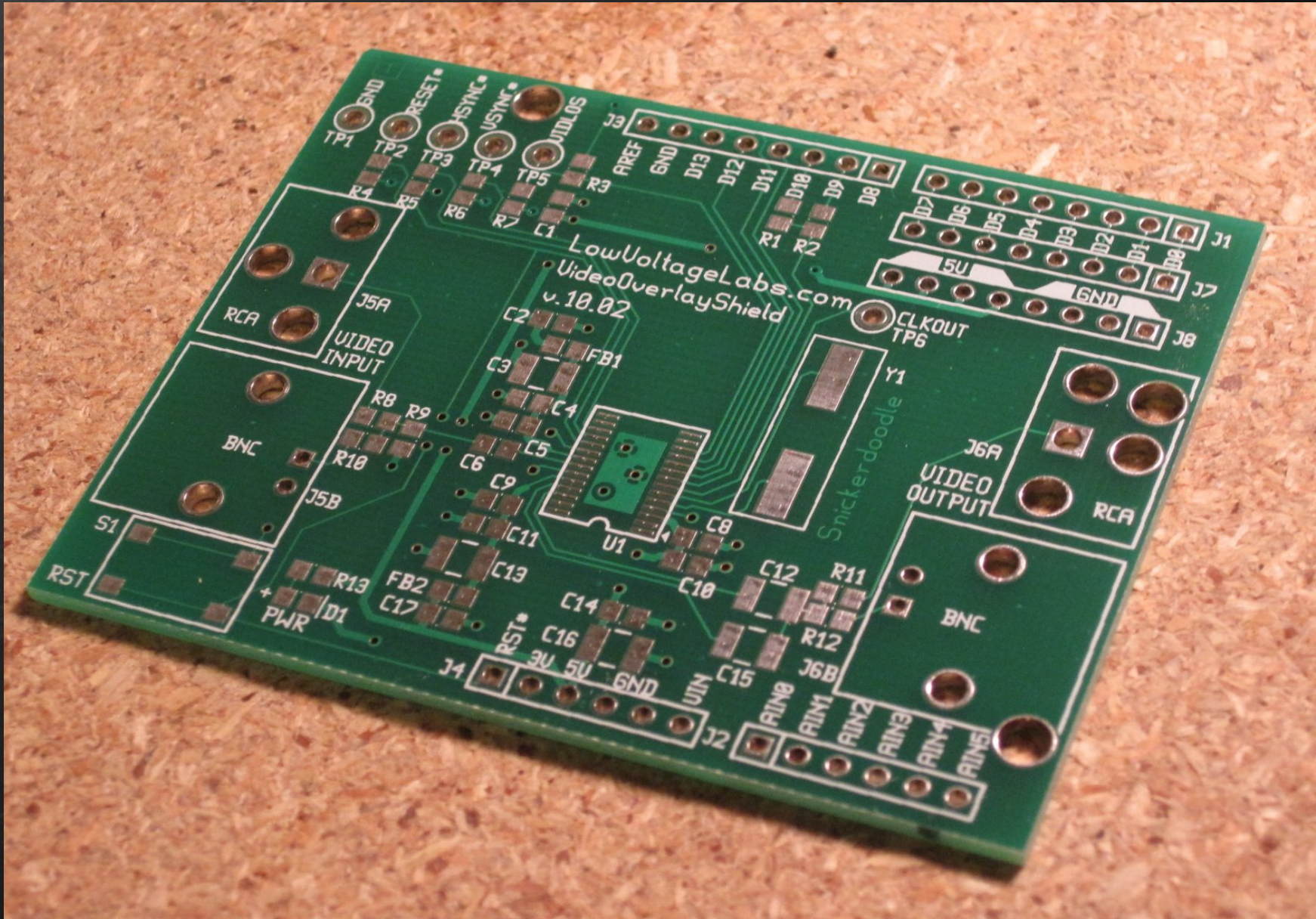


Eric Thompson
LowVoltageLabs.com

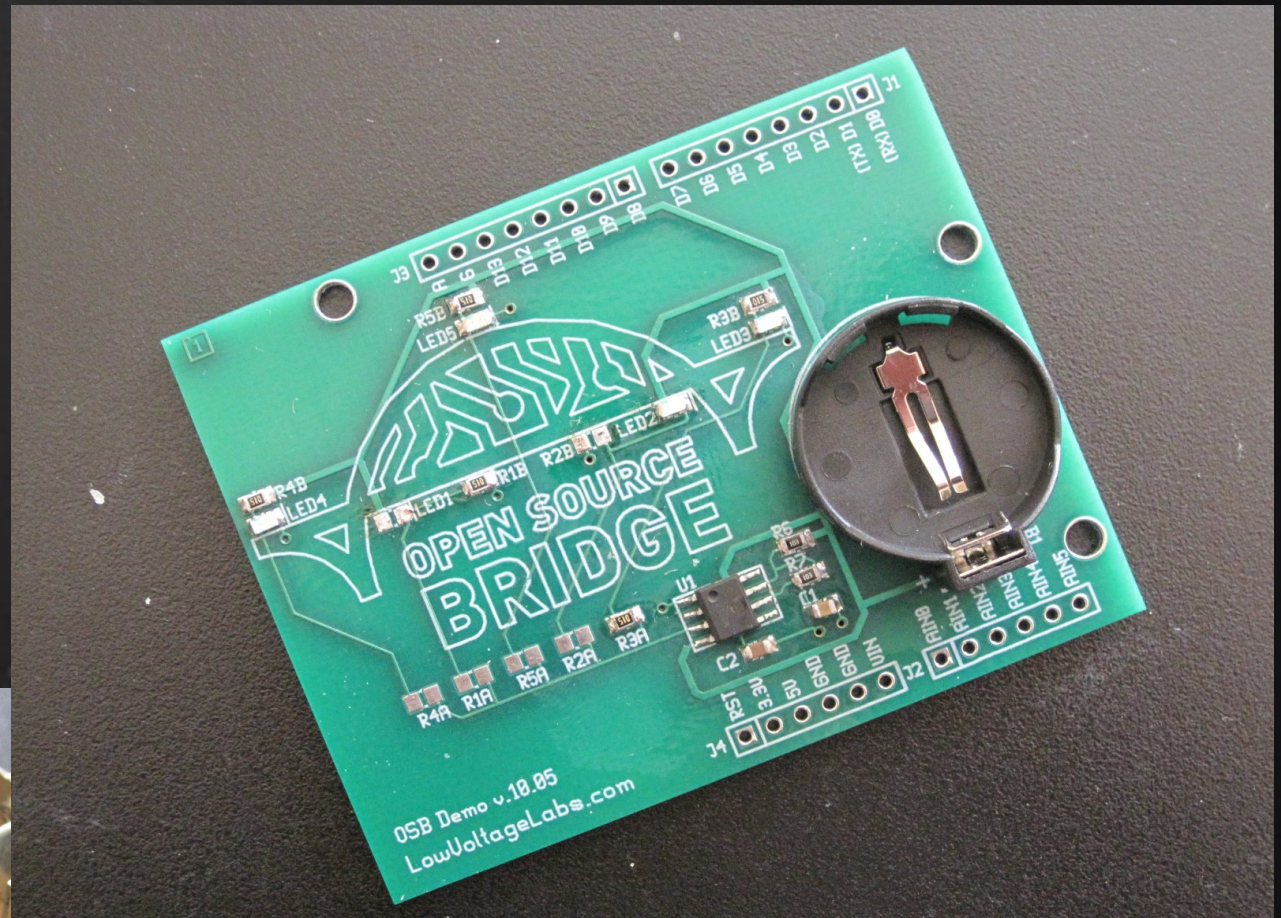
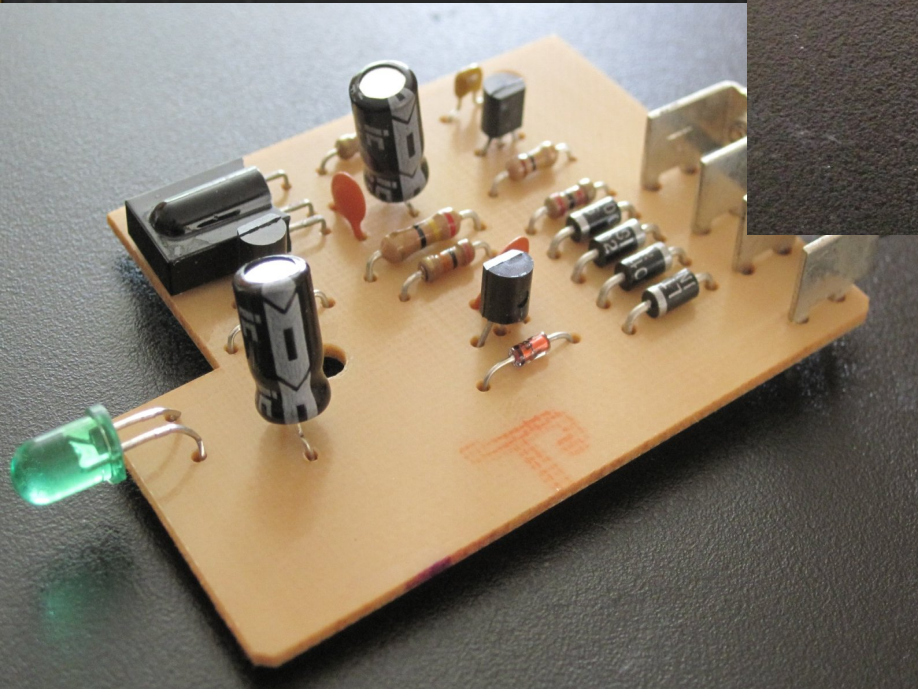
Create a board with KiCAD

- What is a PCB?
- What is a KiCAD?
- Block diagram
- Schematic
- Schematic attribute editor
- Error check the schematic
- PCB layout
- Error check the layout
- Gerber files
- Build boards

What is a printed circuit board (PCB)?



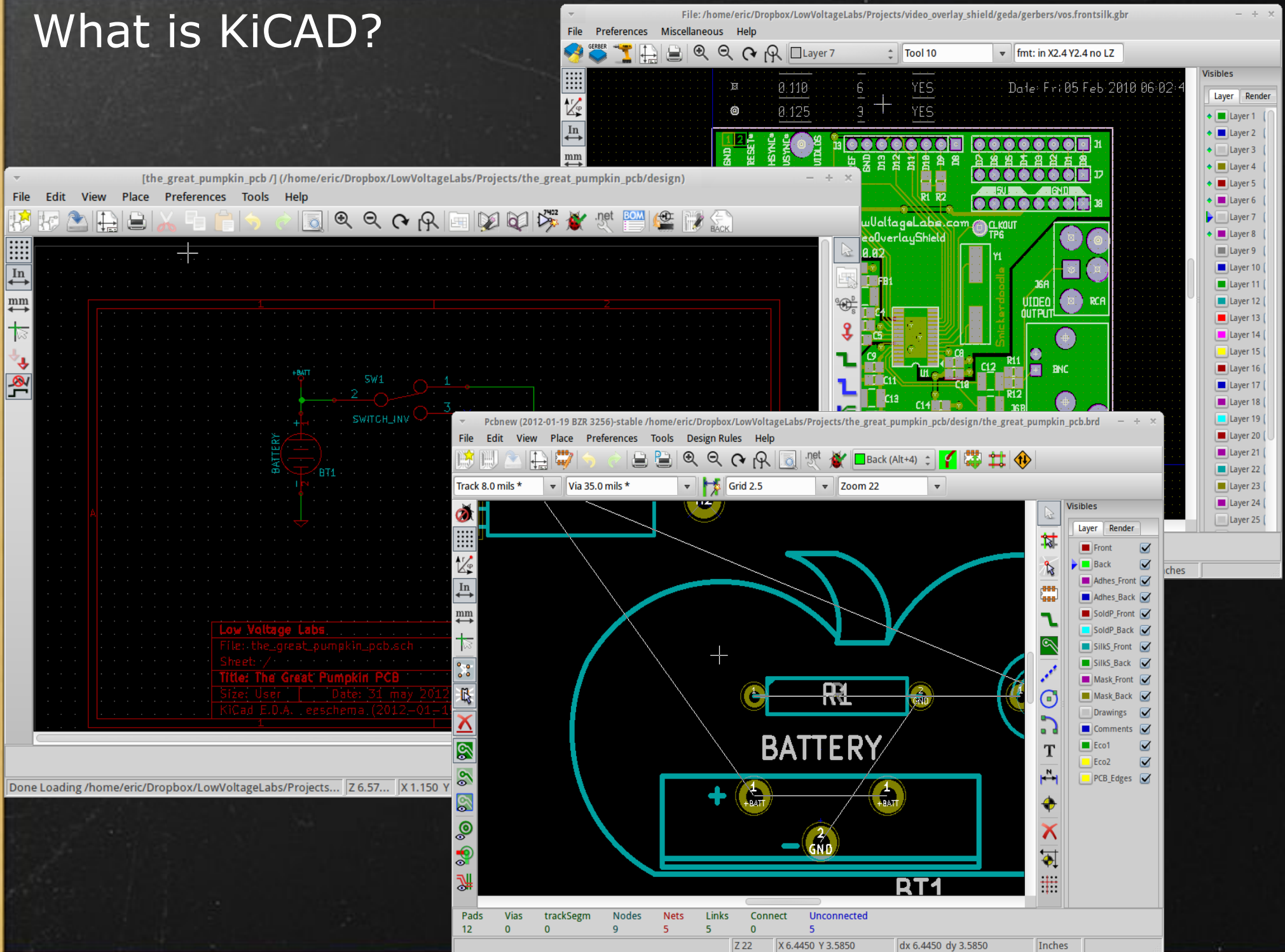
What is a PCB made of?



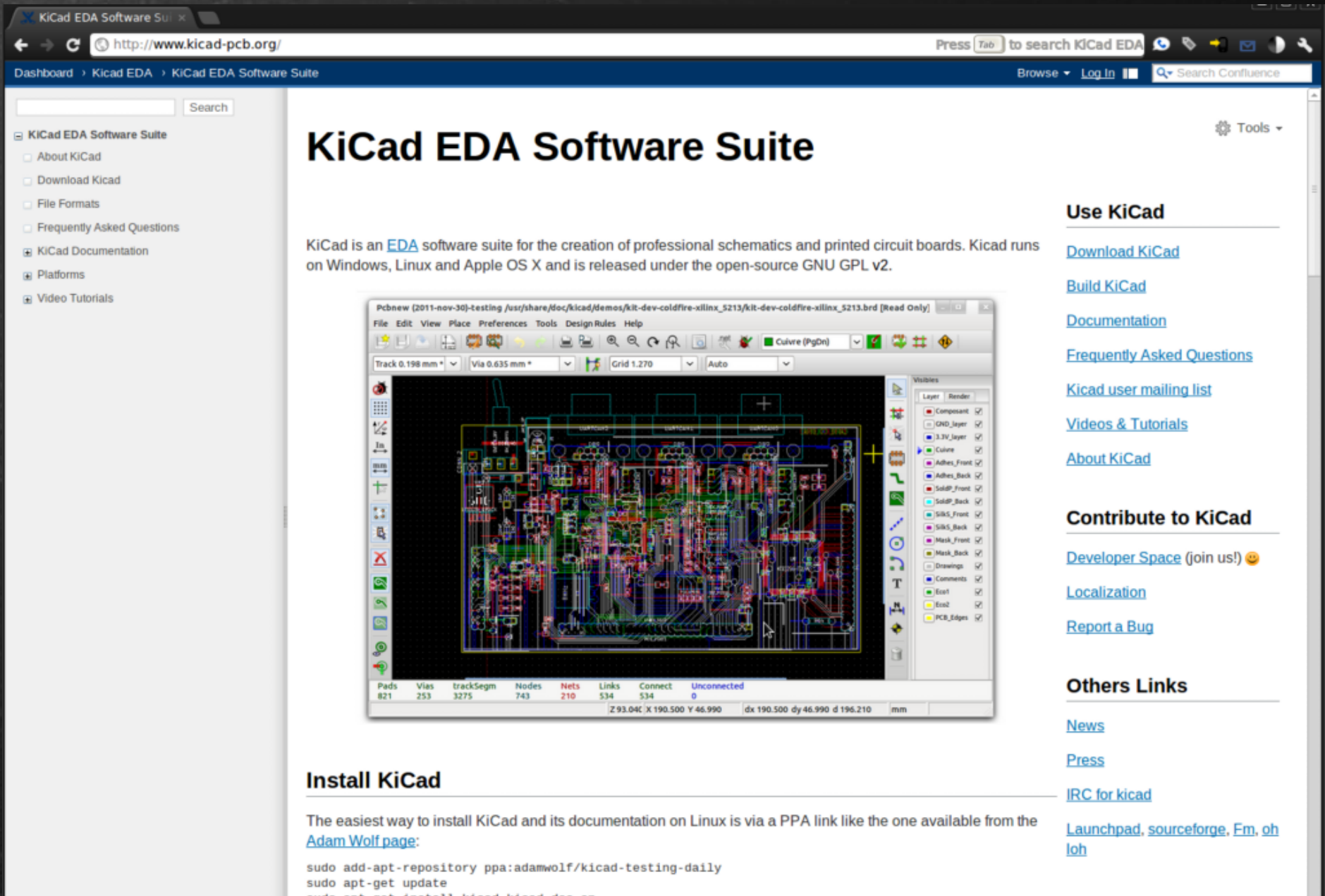
Create a board with KiCAD

- What is a PCB?
- What is a KiCAD?
- Block diagram
- Schematic
- Schematic attribute editor
- Error check the schematic
- PCB layout
- Error check the layout
- Gerber files
- Build boards

What is KiCAD?

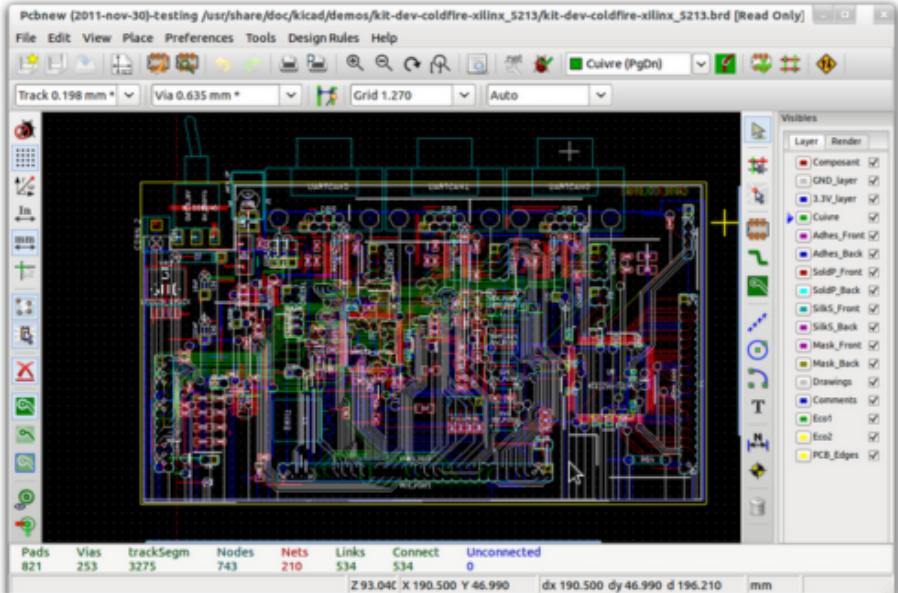


KiCAD website -> <http://www.kicad-pcb.org/>



KiCad EDA Software Suite

KiCad is an [EDA](#) software suite for the creation of professional schematics and printed circuit boards. Kicad runs on Windows, Linux and Apple OS X and is released under the open-source GNU GPL v2.



Pads	Vias	trackSegm	Nodes	Nets	Links	Connect	Unconnected
821	253	3275	743	210	534	534	0

Z 93.04c X 190.500 Y 46.990 dx 190.500 dy 46.990 d 196.210 mm

Use KiCad

- [Download KiCad](#)
- [Build KiCad](#)
- [Documentation](#)
- [Frequently Asked Questions](#)
- [Kicad user mailing list](#)
- [Videos & Tutorials](#)
- [About KiCad](#)

Contribute to KiCad

- [Developer Space](#) (join us!) 😊
- [Localization](#)
- [Report a Bug](#)

Others Links

- [News](#)
- [Press](#)
- [IRC for kicad](#)
- [Launchpad, sourceforge, Fm, oh loh](#)

Install KiCad

The easiest way to install KiCad and its documentation on Linux is via a PPA link like the one available from the [Adam Wolf page](#):

```
sudo add-apt-repository ppa:adamwolf/kicad-testing-daily
sudo apt-get update
sudo apt-get install kicad kicad-doc-en
```

Create a board with KiCAD

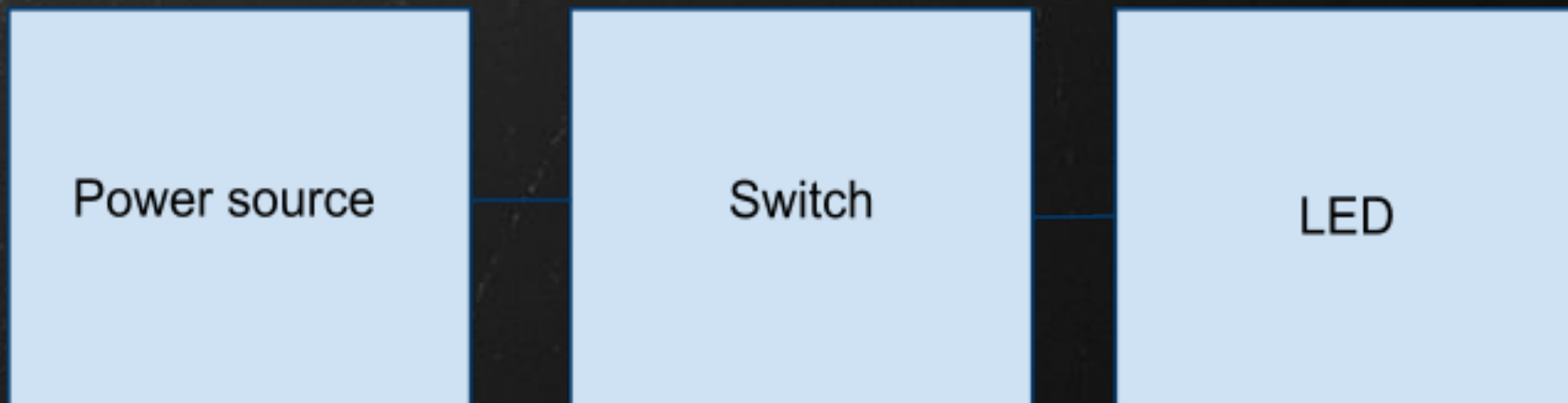
- What is a PCB?
- What is a KiCAD?
- **Block diagram**
- Schematic
- Schematic attribute editor
- Error check the schematic
- PCB layout
- Error check the layout
- Gerber files
- Build boards

Idea:

Create a PCB for the flickering LEDs available from the Evil Mad Science shop.

<http://www.evilmadscientist.com/article.php/simplepumpkins>

Block diagram



Create a board with KiCAD

- What is a PCB?
- What is a KiCAD?
- Block diagram
- **Schematic**
- Schematic attribute editor
- Error check the schematic
- PCB layout
- Error check the layout
- Gerber files
- Build boards

File Browse Preferences Help



▼ **noname.pro**

Empty project



Working dir: /home/eric
Project: noname.pro



Create New Project

Name:

Save in folder: eric Dropbox LowVoltageLabs Projects the_great_pumpkin_pcb design

Places	Name	Size	Modified
Search			
Recently Used			
eric			
Desktop			
File System			
27 GB Filesystem			
Lenovo_Recovery			
Windows7_OS			
SYSTEM_DRV			
Documents			
Download			
Music			
Pictures			
Videos			
Clients			
	the_great_pumpkin_pcb.pro	1.5 KB	Yesterday at 13:43

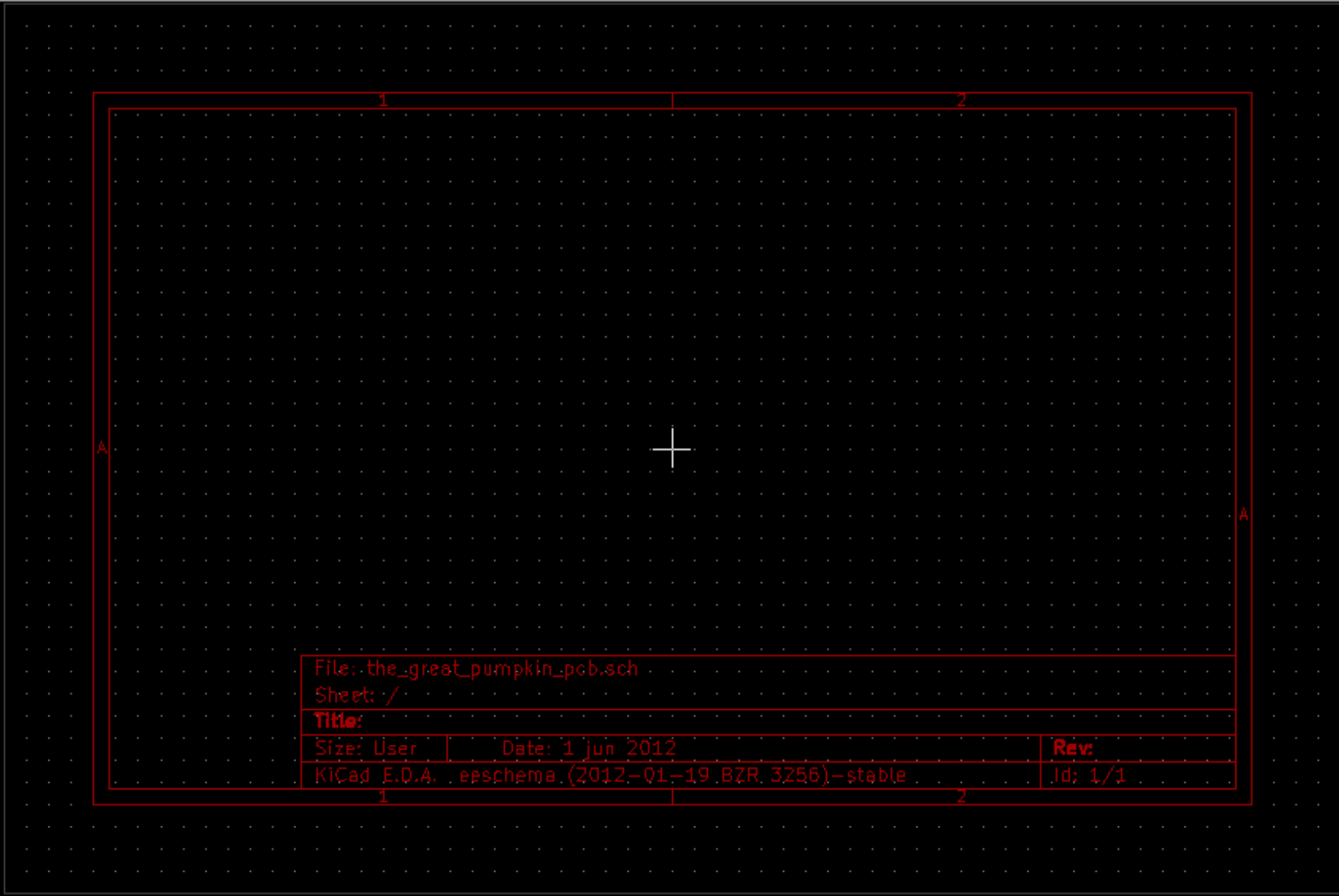
KiCad project files (*.pro)



- the_great_pumpkin_pcb.pro
- the_great_pumpkin_pcb.brd
- the_great_pumpkin_pcb.net
- the_great_pumpkin_pcb.sch



Working in Eeschema (Schematic editor) at /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design
Project: the_great_pumpkin_pcb.pro



File: the_great_pumpkin_pcb.sch		
Sheet: /		
Title:		
Size: User	Date: 1 jun 2012	Rev:
KiCad E.D.A. epschema (2012-01-19 BZR 3256) - stable		.Id: 1/1



Page Settings

Page Size:

- Size A4
- Size A3
- Size A2
- Size A1
- Size A0
- Size A
- Size B
- Size C
- Size D
- Size E
- User size

User Page Size X:

6.000

User Page Size Y:

4.000

Number of sheets: 1 Sheet number: 1

Revision:

1

Export to other sheets

Title:

The Great Pumpkin PCB

Export to other sheets

Company:

Low Voltage Labs

Export to other sheets

Comment1:

Export to other sheets

Comment2:

Export to other sheets

Comment3:

Export to other sheets

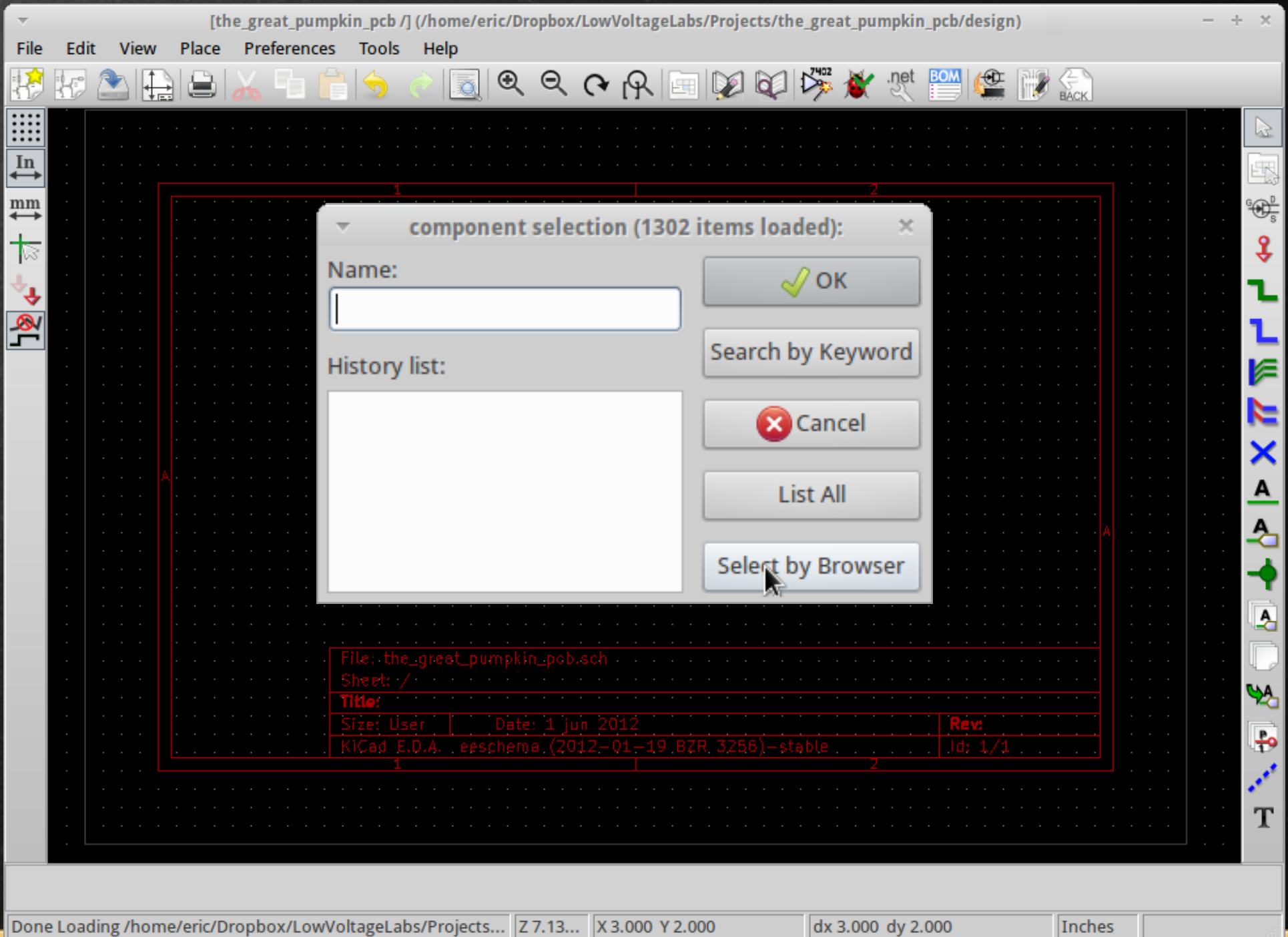
Comment4:

Export to other sheets

Cancel

OK

Add a component with shift-a





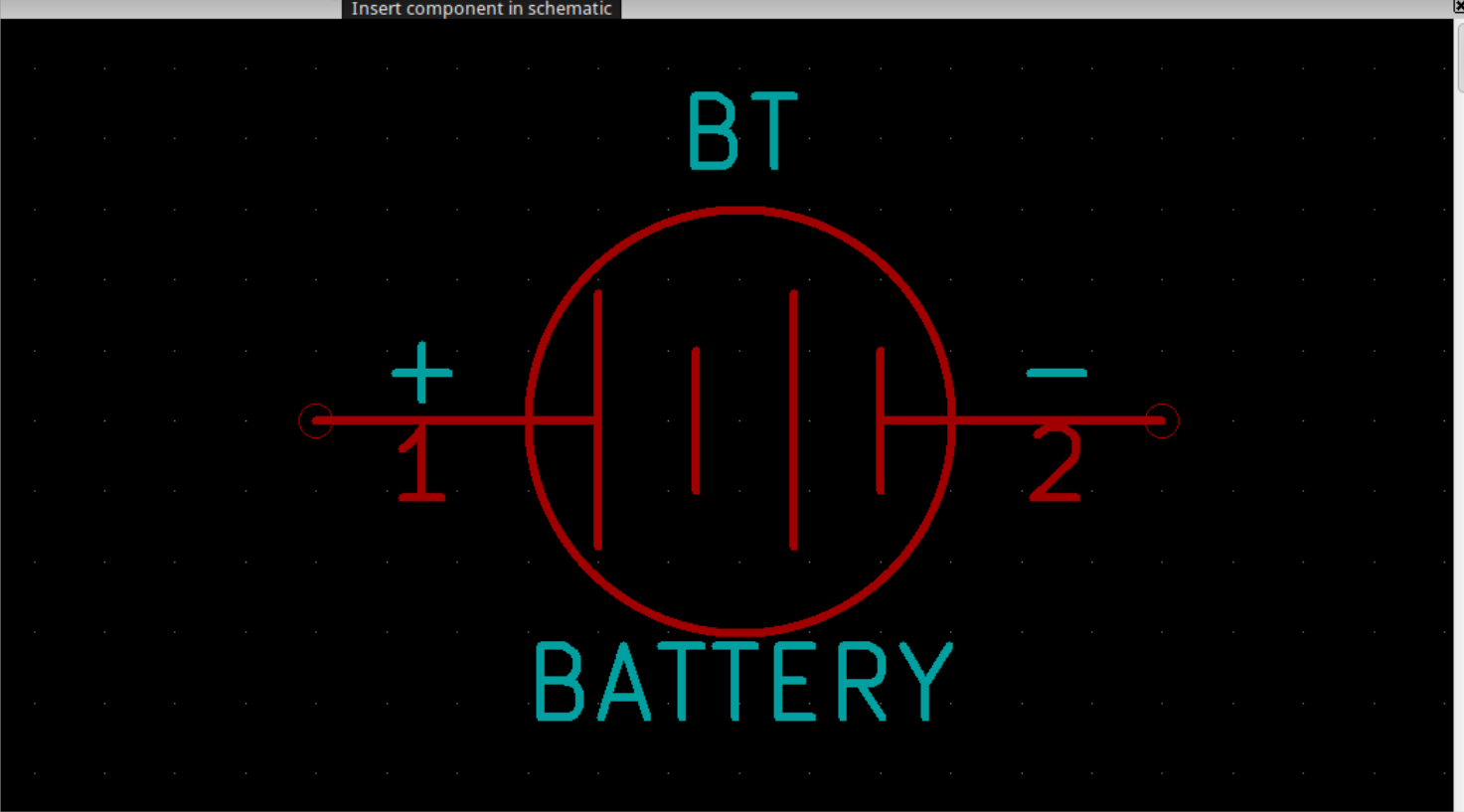
Part A



Insert component in schematic

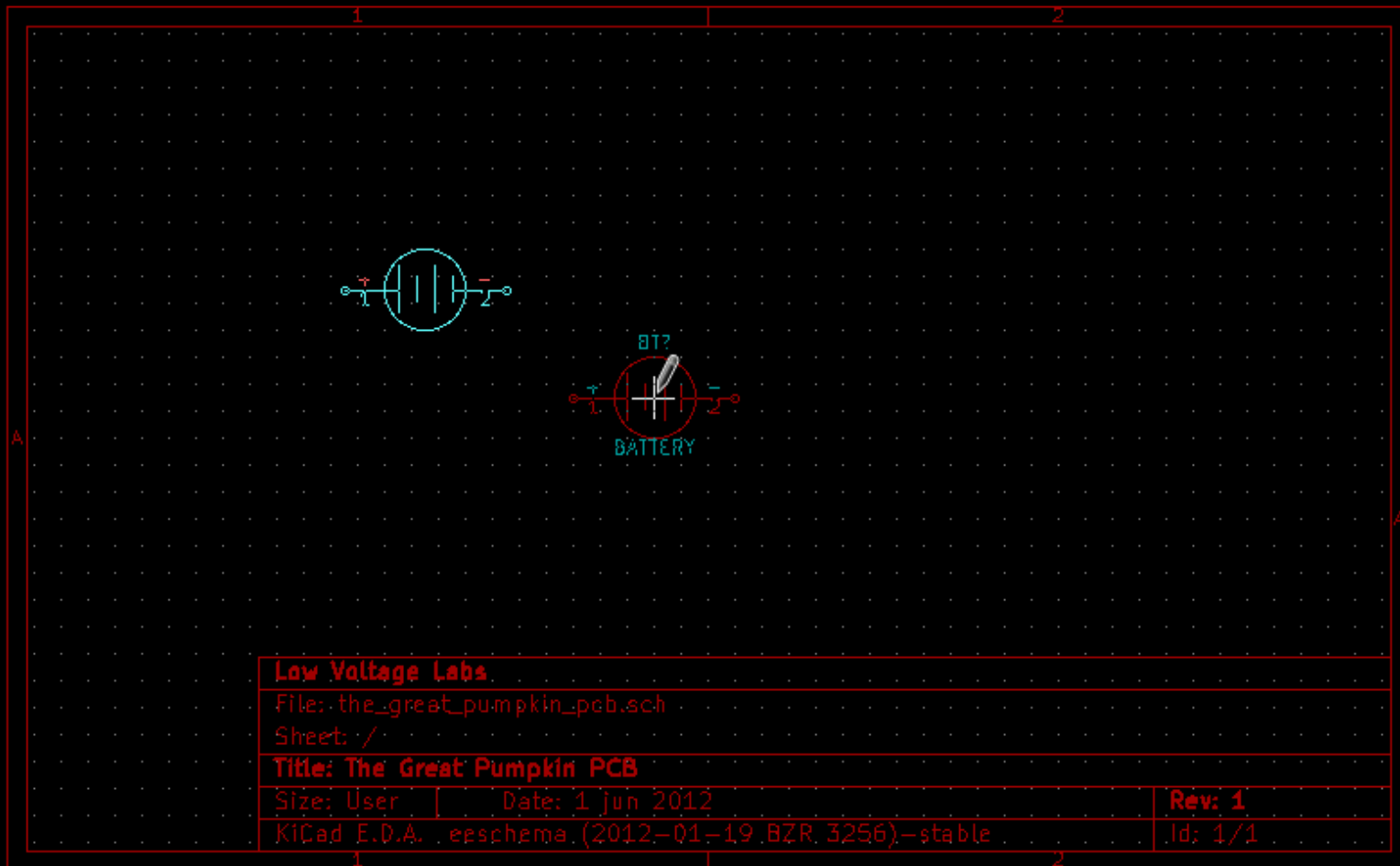
- contrib
- cypress
- device
- digital-audio
- display
- dsp
- intel
- interface
- linear
- memory
- microchip
- microcontrollers
- motorola
- opto
- philips
- power
- regul
- siliconi
- special
- texas
- tgp_pcb
- transistors
- valves
- xilinx
- the_great_pumpkin_

- BATTERY
- BI_LED
- BNC
- BREAKER
- BRIDGE
- C
- CAPAPOL
- CERAMIC_FILTER
- CODING_SWITCH
- CONNECTOR
- CP
- CP1
- CPSMALL
- CRYSTAL
- CSMALL
- CTRIM
- DARL_N
- DIODE
- DIODESCH
- DISPLAY
- DISPLAY_3_LIGNE
- DISPLAY_BL
- DOUBLE_LED
- DOUBLE_SCHOTTKY
- DOUBLE_SCH_KCOM



Part	Alias	Description	Key words
BATTERY	None		

Z 0.99... X -0.300 Y -0.300 dx -0.300 dy -0.300



Low Voltage Labs		
File: the_great_pumpkin_pcb.sch		
Sheet: /		
Title: The Great Pumpkin PCB		
Size: User	Date: 1 jun 2012	Rev: 1
KiCad E.D.A. epschema. (2012-01-19 BZR. 3256)-stable		.Id: 1/1

Reference	Name	Component	Library	Description	Key words
BT?	BATTERY	BATTERY	tgp_pcb		

Done Loading /home/eric/Dropbox/LowVoltageLabs/Projects... Z 6.66... X 2.800 Y 1.850 dx 2.800 dy 1.850 Inches Add compo...

Component editor

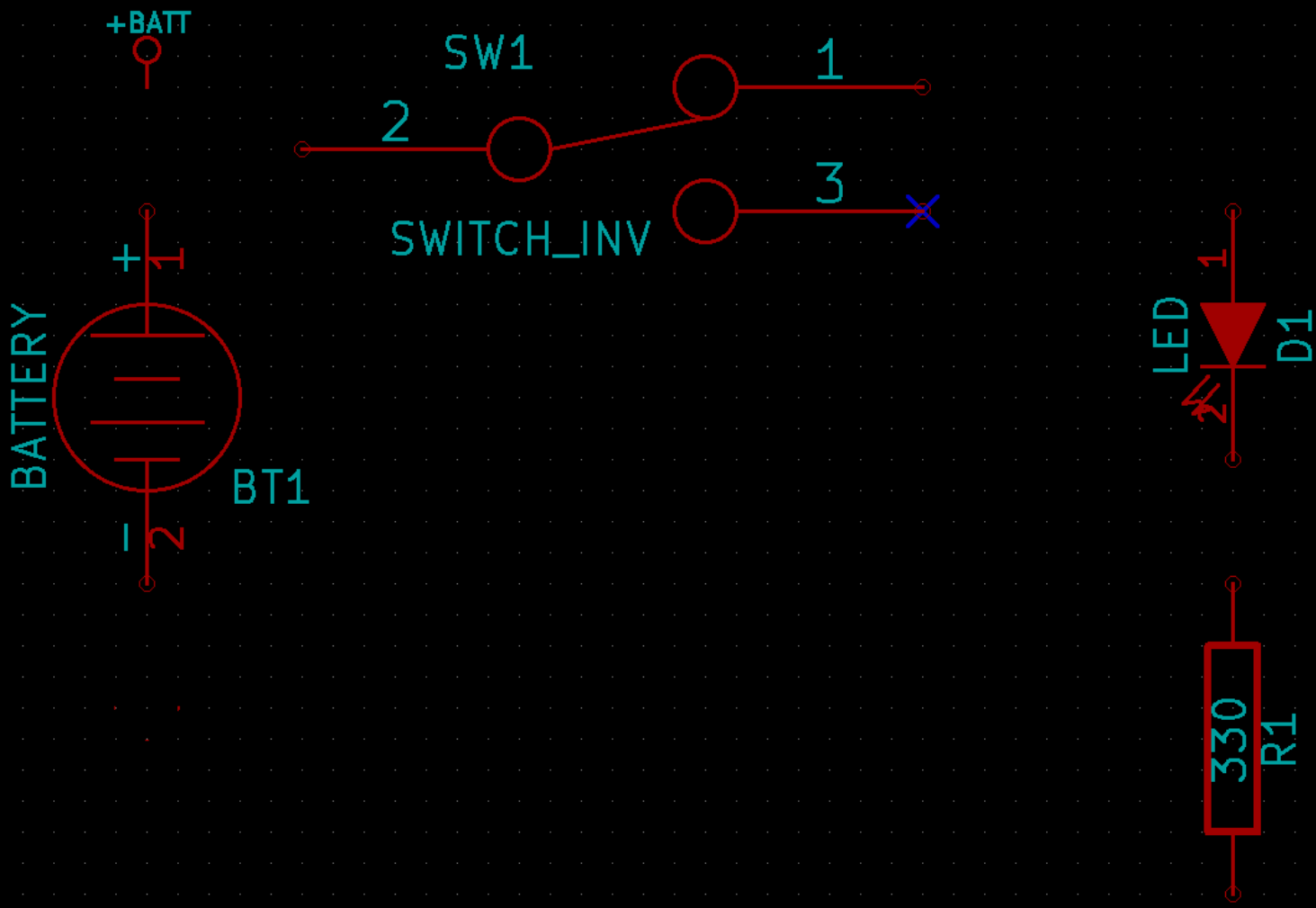
Component Library Editor: /usr/local/kicad/share/library/device.lib

File Edit View Place Preferences Help

The diagram shows a battery symbol in red. It consists of a central circle containing three vertical lines of varying lengths. To the left of the circle is a '+' sign and the number '1'. To the right is a '-' sign and the number '2'. The text 'BT?' is written in cyan above the circle, and 'BATTERY' is written in cyan below it. The symbol is centered on a blue grid.

Part	Alias	Unit	Body	Type	Description	Key words	Datasheet
BATTERY	None	A	Normal	Component			

Z 0.8... X -0.250 Y 0.150 dx -0.250 dy 0.150 Inches



Reference	Power symbol	Component	Library	Description	Key words
#PWR01	GND	GND	power		

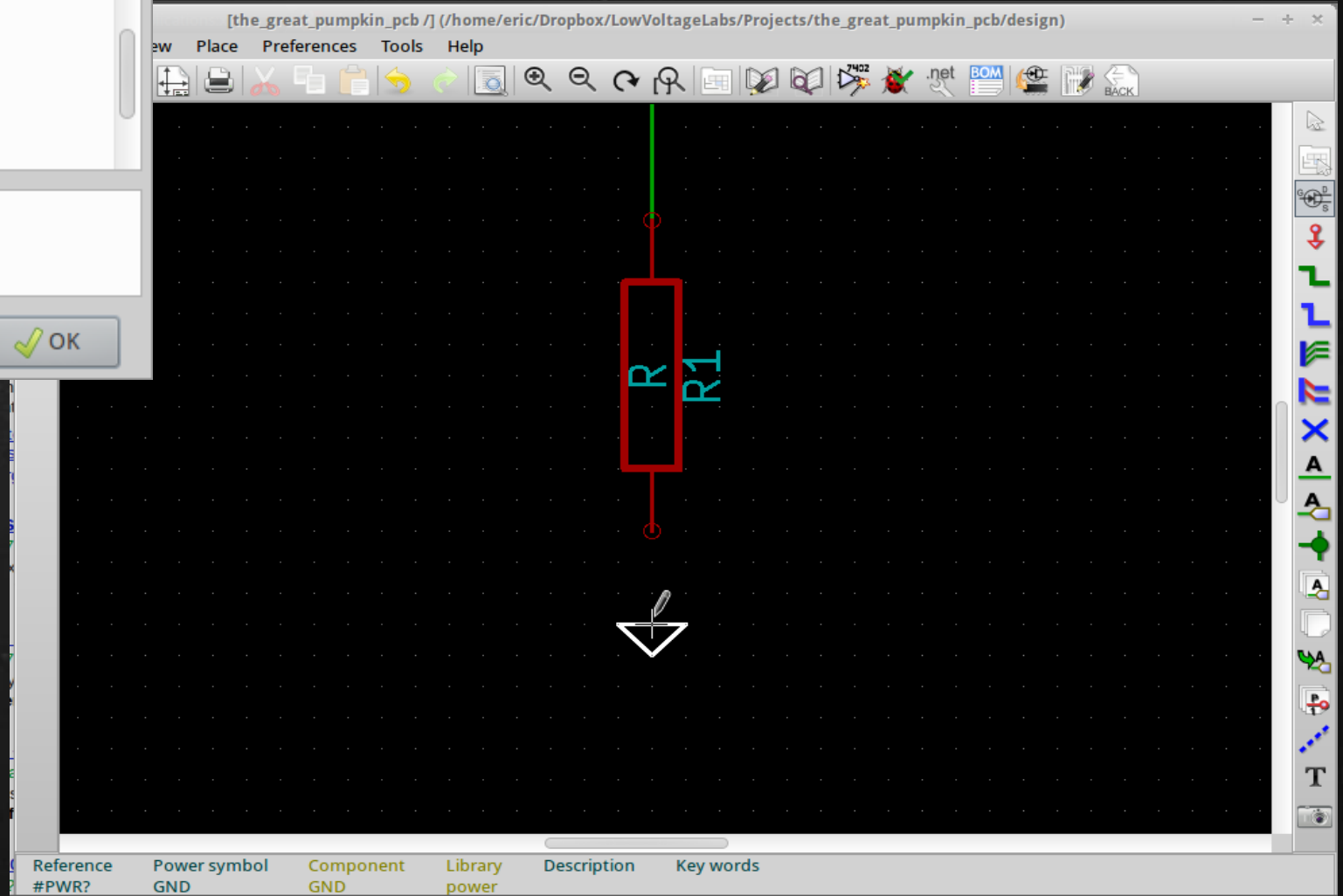
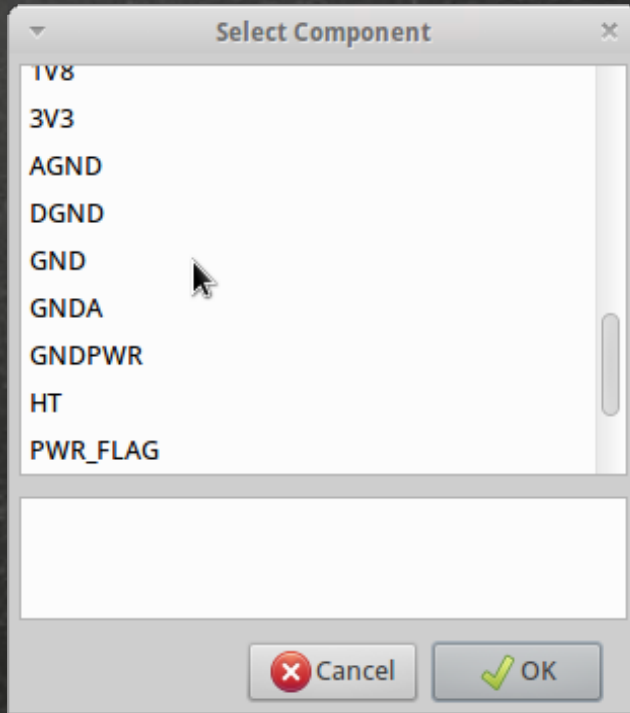
Add wires with shift-w

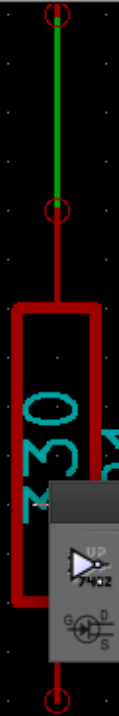
The screenshot shows a circuit design software window titled "[the_great_pumpkin_pcb /] (/home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design)". The window contains a schematic diagram on a dark grid background. The diagram includes a battery symbol labeled "BATTERY" and "BT1" with a positive terminal (+) and a negative terminal (-). A switch symbol labeled "SW1" is connected to the positive terminal. A second switch symbol labeled "SWITCH_INV" is connected to the output of the first switch. The circuit is drawn with red lines and circles. The window has a menu bar (File, Edit, View, Place, Preferences, Tools, Help) and a toolbar with various icons. On the left side, there are vertical toolbars for grid settings, zoom, and units. On the right side, there is a vertical toolbar with various symbols. At the bottom, there is a component list table and a status bar.

Reference	Power symbol	Component	Library	Description	Key words
#PWR1	+BATT	+BATT	power		

Done Loading /home/eric/Dropbox/LowVoltageLabs/Projects... | Z 2 | X 2.150 Y 1.150 | dx 2.150 dy 1.150 | Inches | Add wire

Placing power and GND symbols, shift-P





- Clarify Selection
- Field Value
- Component R, R1

Component Properties



Options

Unit

1

Orientation (Degrees)

0

+90

180

-90

Mirror

Normal

Mirror ---

Mirror |

Chip Name

R

Convert

Reset to Library Defaults

Fields

Name	Value
Reference	R1
Value	330
Footprint	R5
Datasheet	

Add Field

Delete Field

Move Up

Text Justification:

Horiz. Justify

Left

Center

Right

Vert. Justify

Bottom

Center

Top

Visibility

Show

Rotate

Style:

Normal

Italic

Bold

Bold Italic

Field Name

Value

Field Value

330

Size ("):

0.050

Pos X ("):

0.000

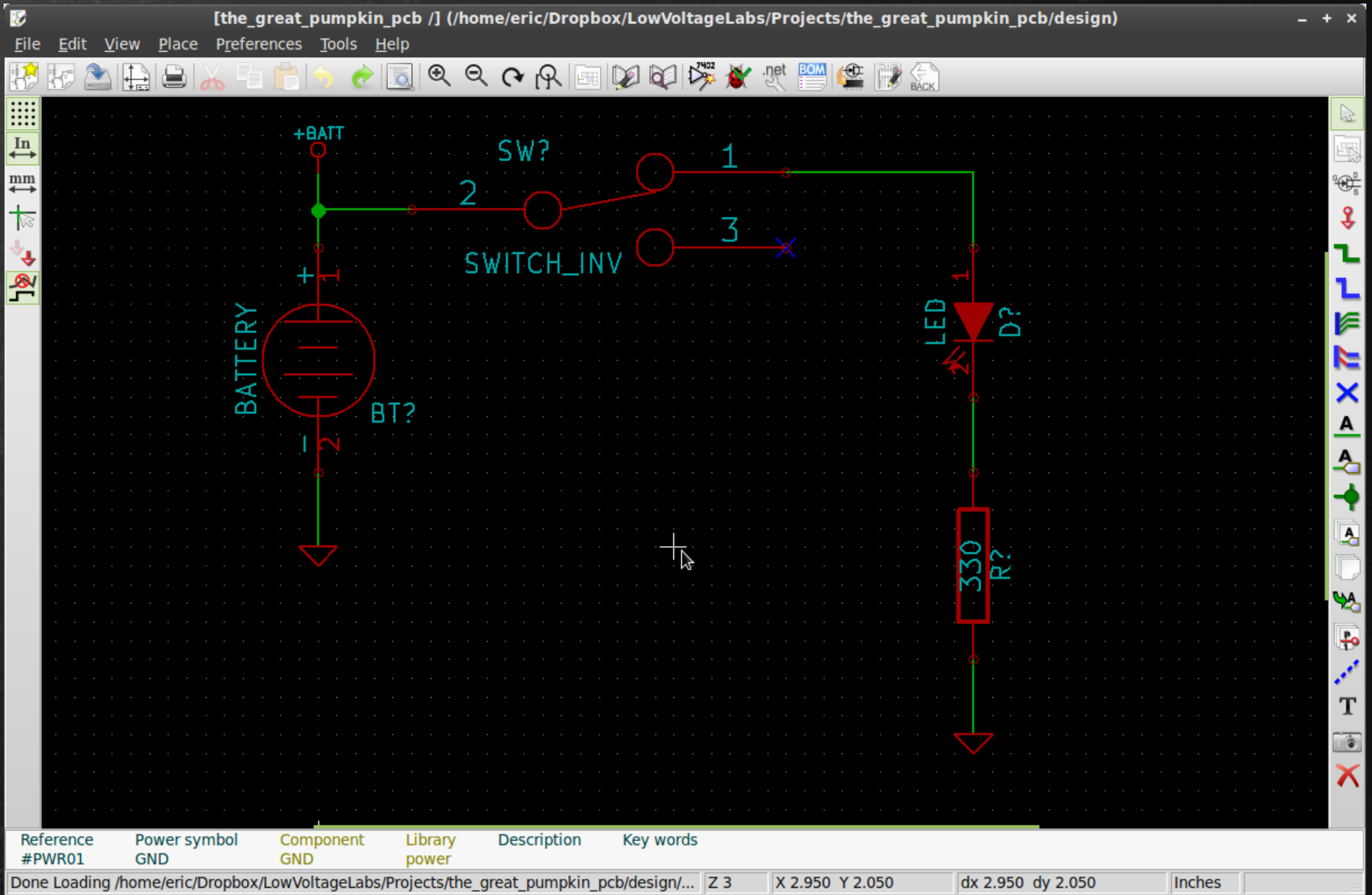
Pos Y ("):

0.000

Cancel

OK

Almost finished with the schematic



Annotate the schematic

The screenshot shows a PCB design software window titled "[the_great_pumpkin_pcb /] (/home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design)". The menu bar includes File, Edit, View, Place, Preferences, Tools, and Help. The Tools menu is open, showing options: Library Browser, Library Editor, Annotate (highlighted), ERC, Generate Netlist, Generate Bill of Materials, Assign Component Footprints, and Layout Printed Circuit Board. The schematic diagram features a battery labeled "BATTERY" with a component ID "BT1", a resistor labeled "330 R1", and an LED labeled "LED D1". Two test points are labeled "1" and "3". The status bar at the bottom displays: "Annotate the components in the schematic", "Z 3", "X 2.100 Y 0.850", "dx 2.100 dy 0.850", and "Inches".

Reference	Power symbol	Component	Library	Description	Key words
#PWR01	GND	GND	power		



Annotate Schematic

Scope

- Use the entire schematic
- Use the current page only

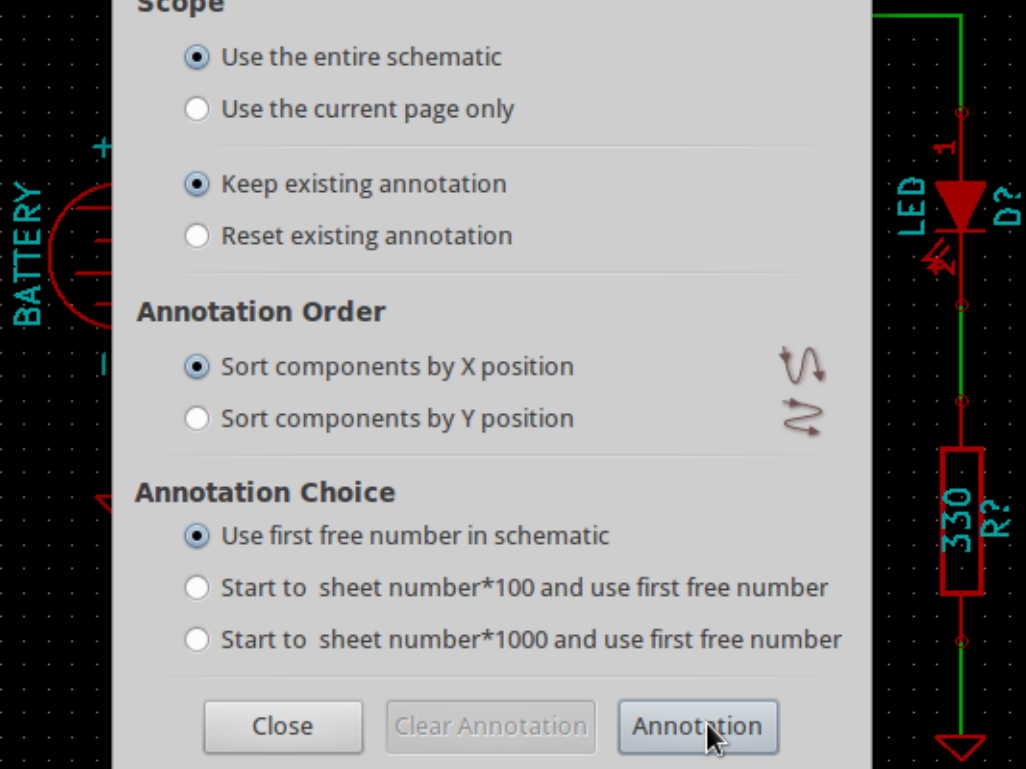
Annotation Order

- Sort components by X position
- Sort components by Y position

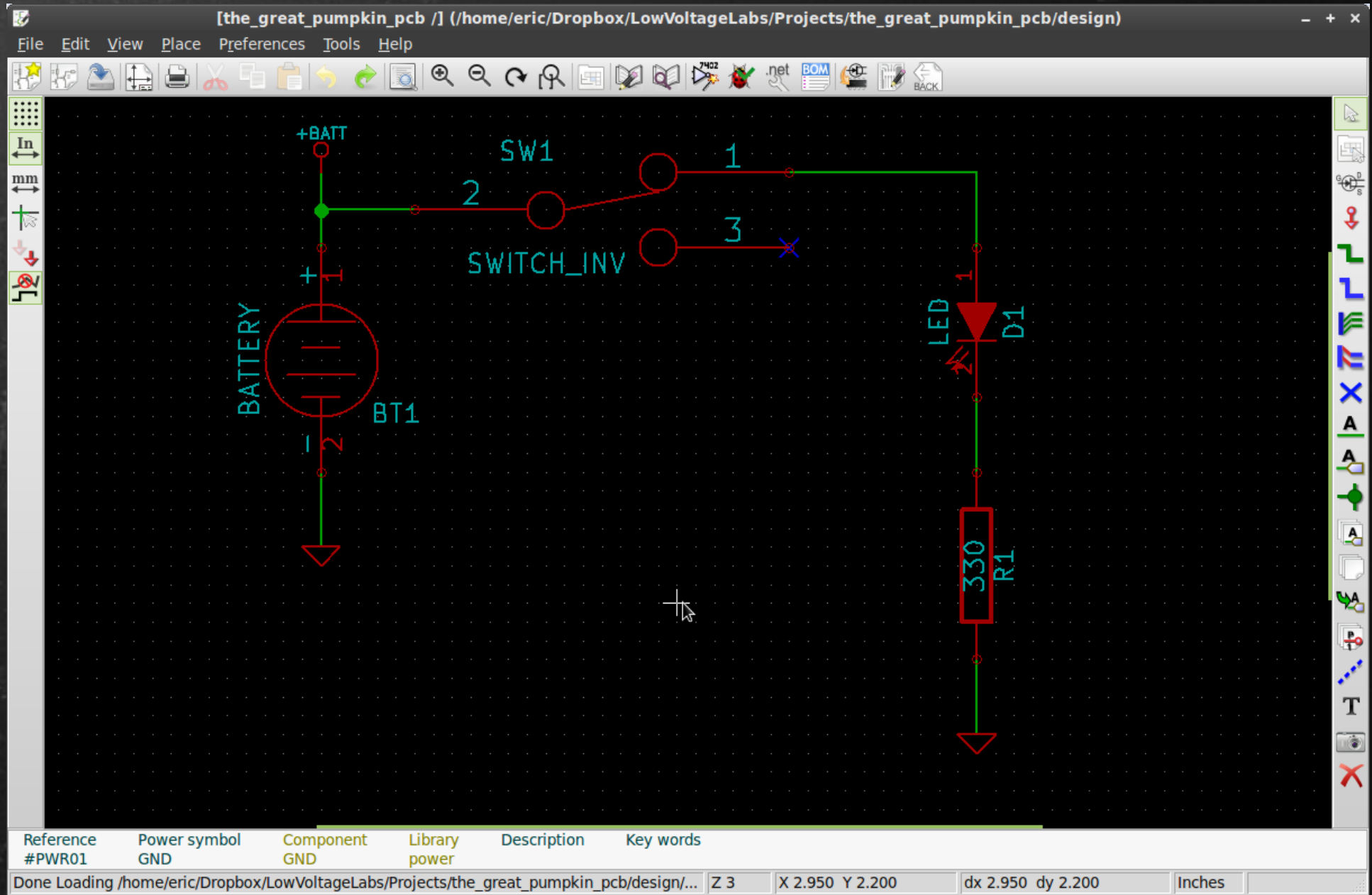
Annotation Choice

- Use first free number in schematic
- Start to sheet number*100 and use first free number
- Start to sheet number*1000 and use first free number

Close Clear Annotation Annotation



Finished schematic



Create a board with KiCAD

- What is a PCB?
- What is a KiCAD?
- Block diagram
- Schematic
- Schematic attribute editor
- Error check the schematic
- PCB layout
- Error check the layout
- Gerber files
- Build boards

Error rule check the schematic

The screenshot shows a PCB design software interface with a schematic diagram and an open 'Tools' menu. The schematic includes a battery component labeled 'BATTERY' and 'BT1', an LED component labeled 'LED' and 'D1', and a resistor component labeled '330' and 'R1'. The 'Tools' menu is open, highlighting the 'ERC' (Electrical Rules Check) option. The status bar at the bottom displays the text 'Perform electrical rule check' and various coordinates and units.

Reference	Power symbol	Component	Library	Description	Key words
#PWR01	GND	GND	power		

Perform electrical rule check Z 3 X 2.350 Y 0.850 dx 2.350 dy 0.850 Inches

EESchema Erc

ERC

Options

Erc File Report:

Total Errors Count: 1

Warnings Count: 1

Errors Count: 0

Messages:

Item not annotated: D?
Annotation required!

Test Erc

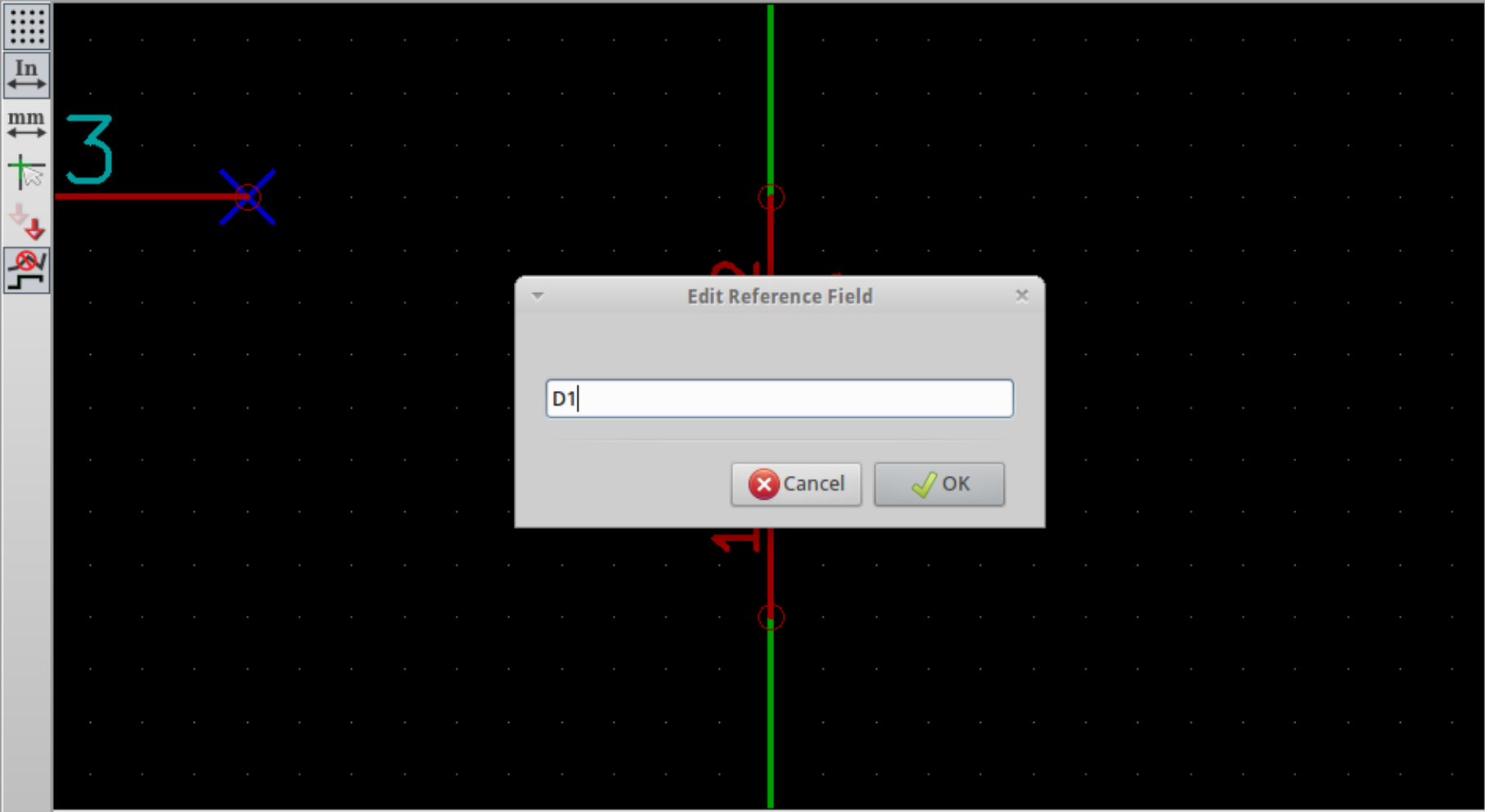
Del Markers

Close

Create ERC report

Markers:

Empty text area for markers.



Dialog box titled "Edit Reference Field" with a text input field containing "D1" and "Cancel" and "OK" buttons.

Reference	Name	Component	Library	Description	Key words
D?	LED	LED	device		LED

EESchema Erc

ERC

Options

Erc File Report:

Total Errors Count: 0

Warnings Count: 0

Errors Count: 0

Messages:

Empty text area for messages.

Test Erc

Del Markers

Close

Create ERC report

Markers:

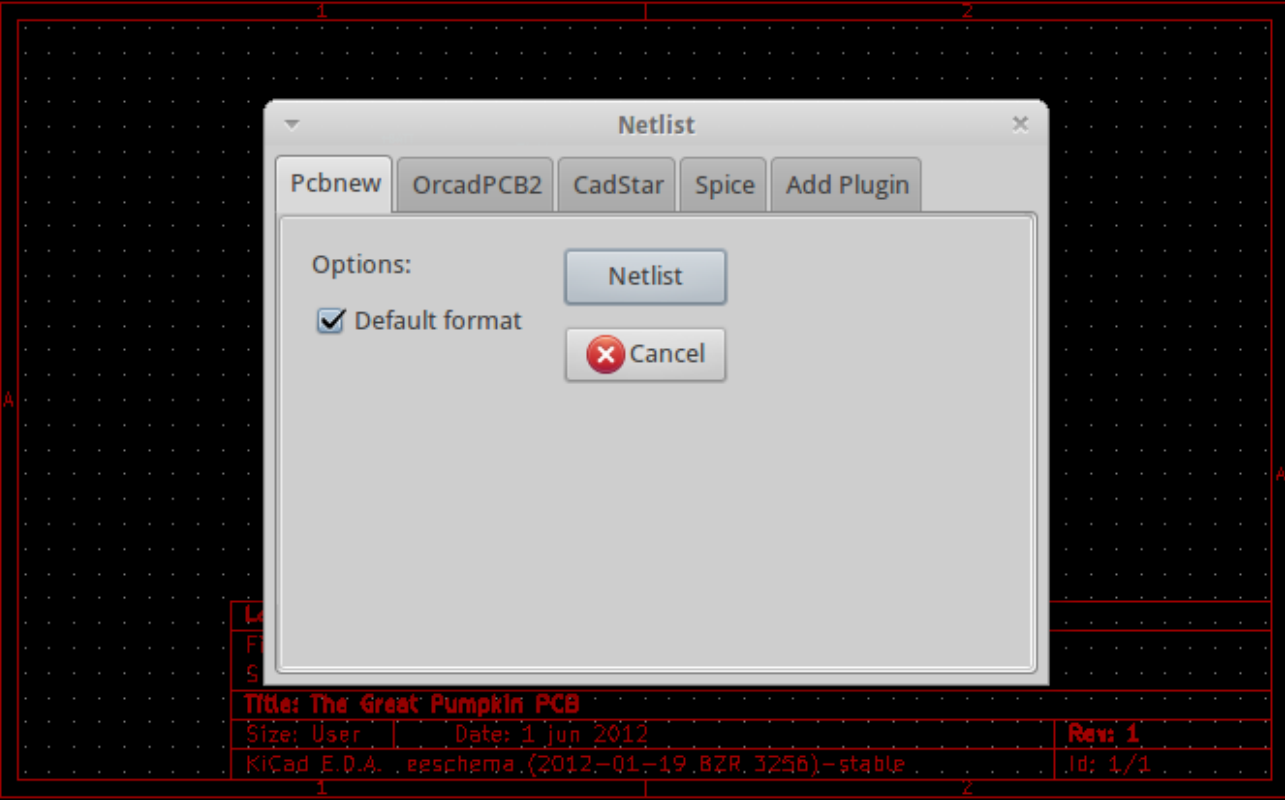
Large empty text area for markers.

Generate a netlist

The screenshot shows a PCB design software window titled "[the_great_pumpkin_pcb /] (/home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design)". The 'Tools' menu is open, with 'Generate Netlist' highlighted. The circuit diagram includes a battery labeled 'BATTERY' and 'BT1', a resistor labeled '330 R1', and an LED labeled 'LED' and 'D1'. The netlist table at the bottom is as follows:

Reference	Power symbol	Component	Library	Description	Key words
#PWR01	GND	GND	power		

At the bottom of the window, there is a status bar with the text "Generate the component netlist" and coordinates: "Z 3", "X 2.050 Y 0.850", "dx 2.050 dy 0.850", and "Inches".



Netlist

Pcbnew | OrcadPCB2 | CadStar | Spice | Add Plugin

Options:

- Default format

Buttons: Netlist, Cancel

Title: The Great Pumpkin PCB		
Size: User	Date: 1 Jun 2012	Rev: 1
KiCad E.D.A. . epschema . (2012-01-19 BZR 3256) - stable		Id: 1/1

Create a board with KiCAD

- What is a PCB?
- What is a KiCAD?
- Block diagram
- Schematic
- Schematic attribute editor - CvPCB
- Error check the schematic
- PCB layout
- Error check the layout
- Gerber files
- Build boards



- the_great_pumpkin_pcb.pro
- the_great_pumpkin_pcb.brd
- the_great_pumpkin_pcb.net
- the_great_pumpkin_pcb.sch



Working dir: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design
Project: the_great_pumpkin_pcb.pro



1	BT1 -	BATTERY : CR2032V
2	D1 -	LED : LED-5MM
3	R1 -	R : R5
4	SW1 -	SPST : SW_SPDT

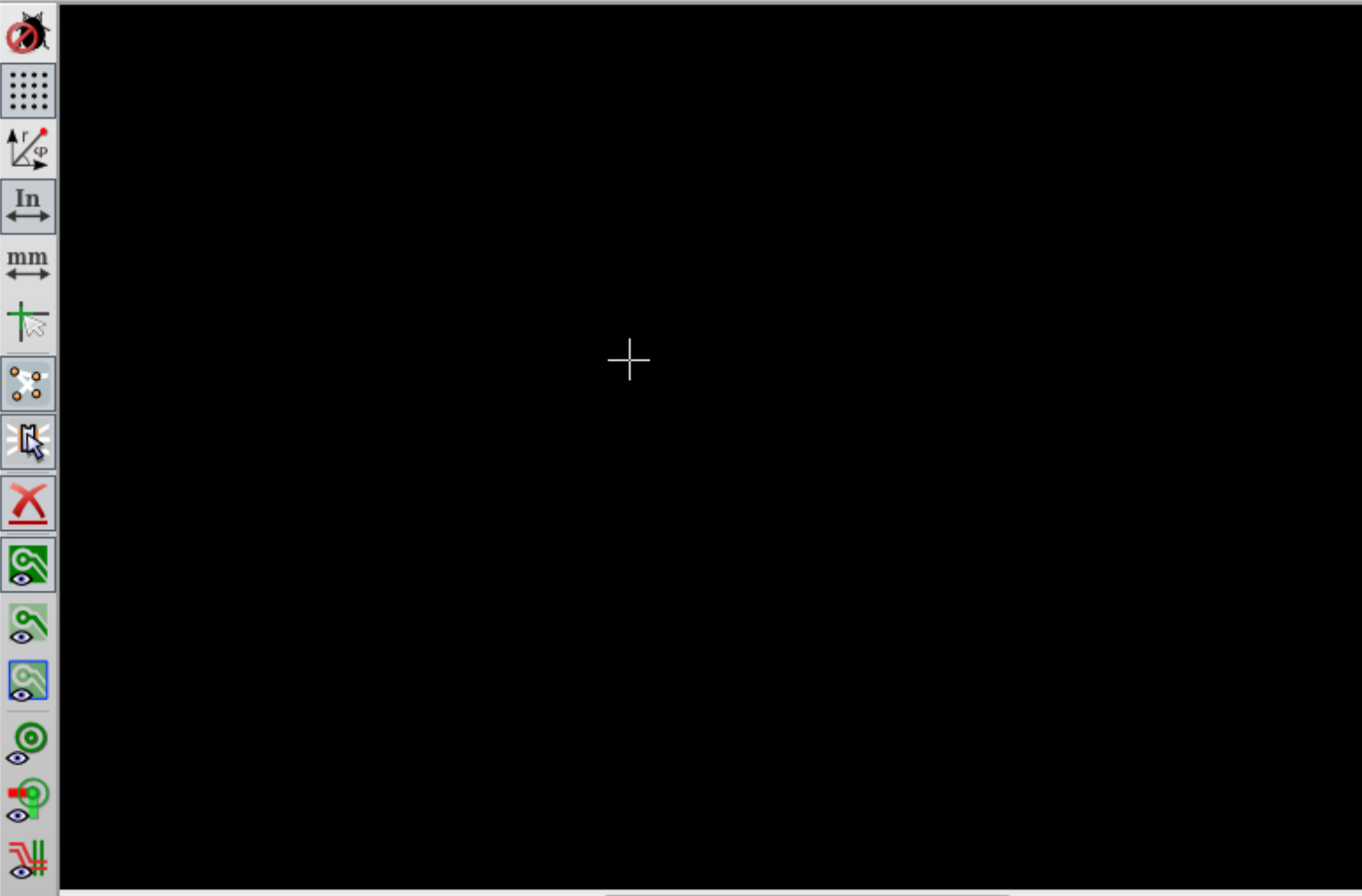
1	1pin
2	1pin
3	2PIN_6mm
4	3M-N7E50
5	3M-N7E50
6	3PIN_6mm
7	8DIPCMS
8	20TEX-ELL300
9	20TEX300
10	24tex300
11	24TEXT-ELL300
12	28TEX-ELL600
13	28tex600
14	40tex-ELL600
15	40tex600
16	80188
17	ADSP2100
18	AFF_2x7SEG-D...
19	AK300-2
20	BGA48
21	BGA64-0.8mm

Create a board with KiCAD

- What is a PCB?
- What is a KiCAD?
- Block diagram
- Schematic
- Schematic attribute editor
- Error check the schematic
- **PCB layout**
- Error check the layout
- Gerber files
- Build boards



Track 8.0 mils * Via 35.0 mils * Grid 2.5 Zoom 50



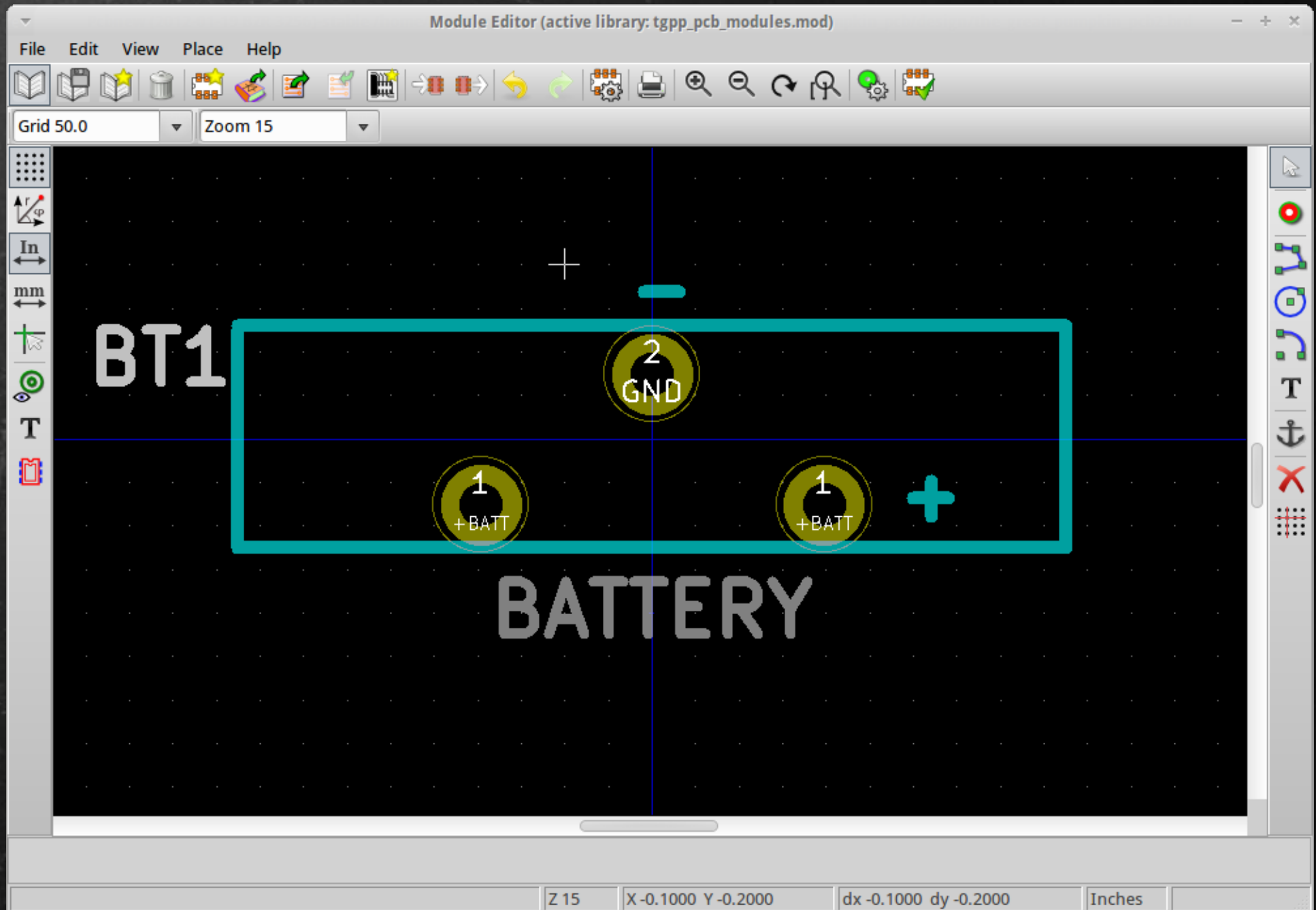
Visibles

Layer	Render
Front	<input checked="" type="checkbox"/>
Back	<input checked="" type="checkbox"/>
Adhes_Front	<input checked="" type="checkbox"/>
Adhes_Back	<input checked="" type="checkbox"/>
SoldP_Front	<input checked="" type="checkbox"/>
SoldP_Back	<input checked="" type="checkbox"/>
Silks_Front	<input checked="" type="checkbox"/>
Silks_Back	<input checked="" type="checkbox"/>
Mask_Front	<input checked="" type="checkbox"/>
Mask_Back	<input checked="" type="checkbox"/>
Drawings	<input checked="" type="checkbox"/>
Comments	<input checked="" type="checkbox"/>
Eco1	<input checked="" type="checkbox"/>
Eco2	<input checked="" type="checkbox"/>
PCB_Edges	<input checked="" type="checkbox"/>

Pads	Vias	trackSegm	Nodes	Nets	Links	Connect	Unconnected
0	0	0	0	1	0	0	0

Z 50 X 6.4400 Y 3.4350 dx 6.4400 dy 3.4350 Inches

PCB module editor



Netlist

The screenshot shows the Pcbnew software interface. The main window title is "Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.brd". The menu bar includes File, Edit, View, Place, Preferences, Tools, Design Rules, and Help. The Tools menu is open, showing options: Netlist, Layer Pair, DRC, and FreeRoute. The Netlist dialog box is open, displaying the following settings:

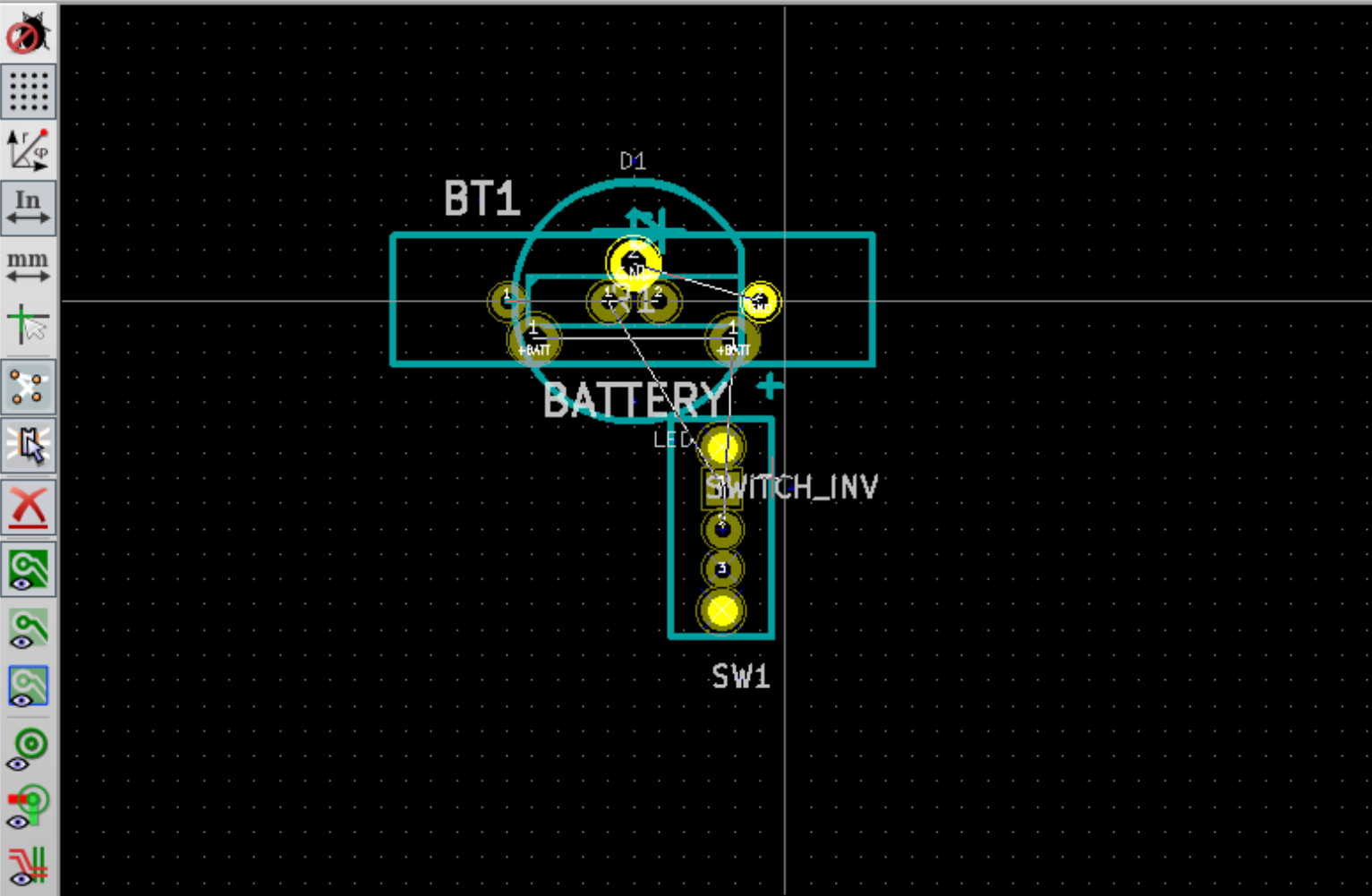
- Module Selection: Reference, Timestamp
- Bad Tracks Deletion: Keep, Delete
- Exchange Module: Keep, Change
- Extra Footprints: Keep, Delete

Buttons in the dialog include: Browse Netlist Files, Read Current Netlist, Footprints Test, Rebuild Board Connectivity, and Close. The Netlist File field contains: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/de. The Messages field is empty.

At the bottom of the Pcbnew window, a status bar shows: Backup file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/t, Wrote board file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/de, Read the netlist and update board connectivity, Z 10, X 5.0250 Y 4.0000.



Track 50.0 mils Via 35.0 mils * Grid 25.0 Zoom 35



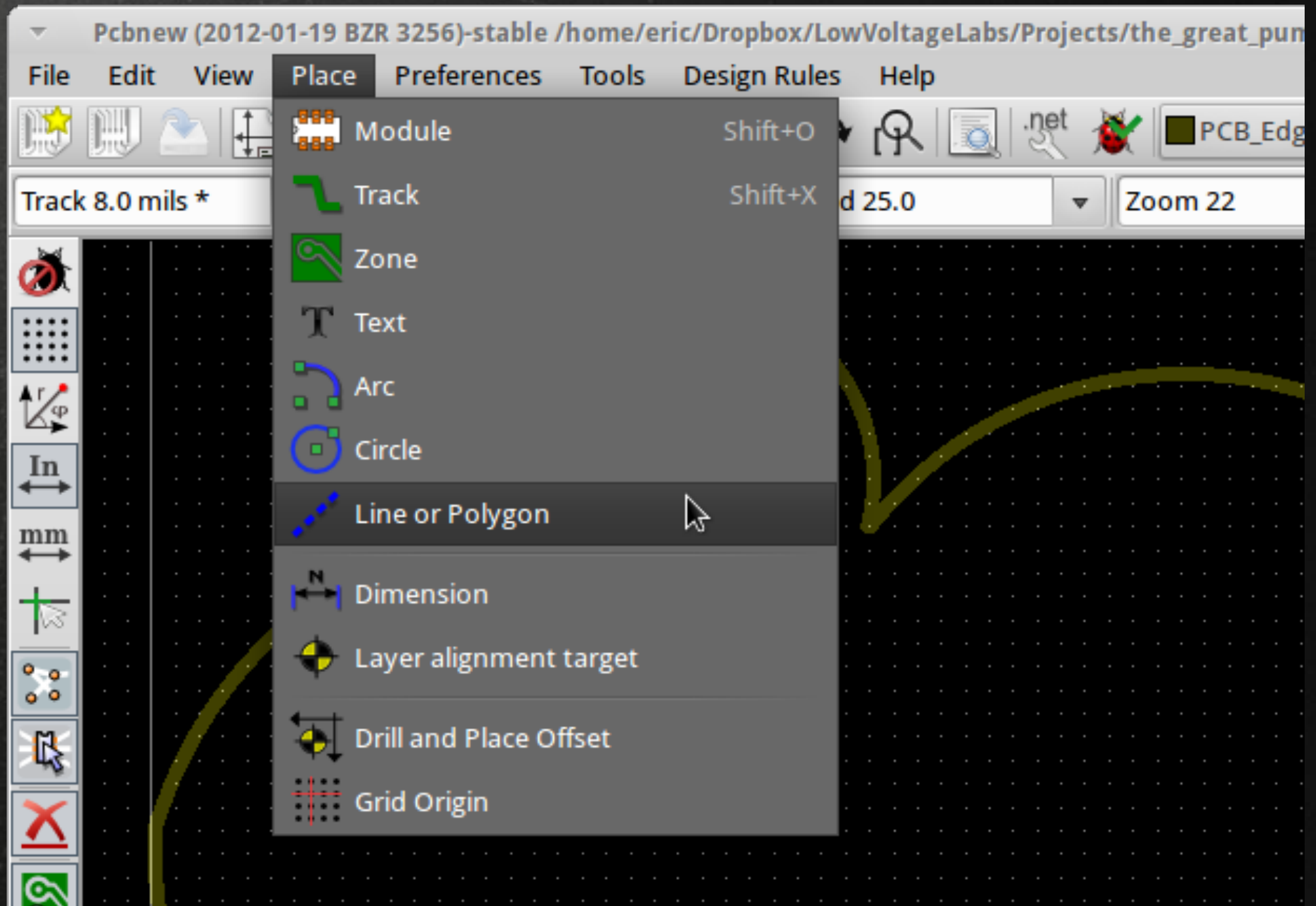
Visibles

Layer	Render
Front	<input checked="" type="checkbox"/>
Back	<input checked="" type="checkbox"/>
Adhes_Front	<input checked="" type="checkbox"/>
Adhes_Back	<input checked="" type="checkbox"/>
SoldP_Front	<input checked="" type="checkbox"/>
SoldP_Back	<input checked="" type="checkbox"/>
Silks_Front	<input checked="" type="checkbox"/>
Silks_Back	<input checked="" type="checkbox"/>
Mask_Front	<input checked="" type="checkbox"/>
Mask_Back	<input checked="" type="checkbox"/>
Drawings	<input checked="" type="checkbox"/>
Comments	<input checked="" type="checkbox"/>
Eco1	<input checked="" type="checkbox"/>
Eco2	<input checked="" type="checkbox"/>
PCB_Edges	<input checked="" type="checkbox"/>

Pads	Vias	trackSegm	Nodes	Nets	Links	Connect	Unconnected
12	0	0	9	5	5	0	5

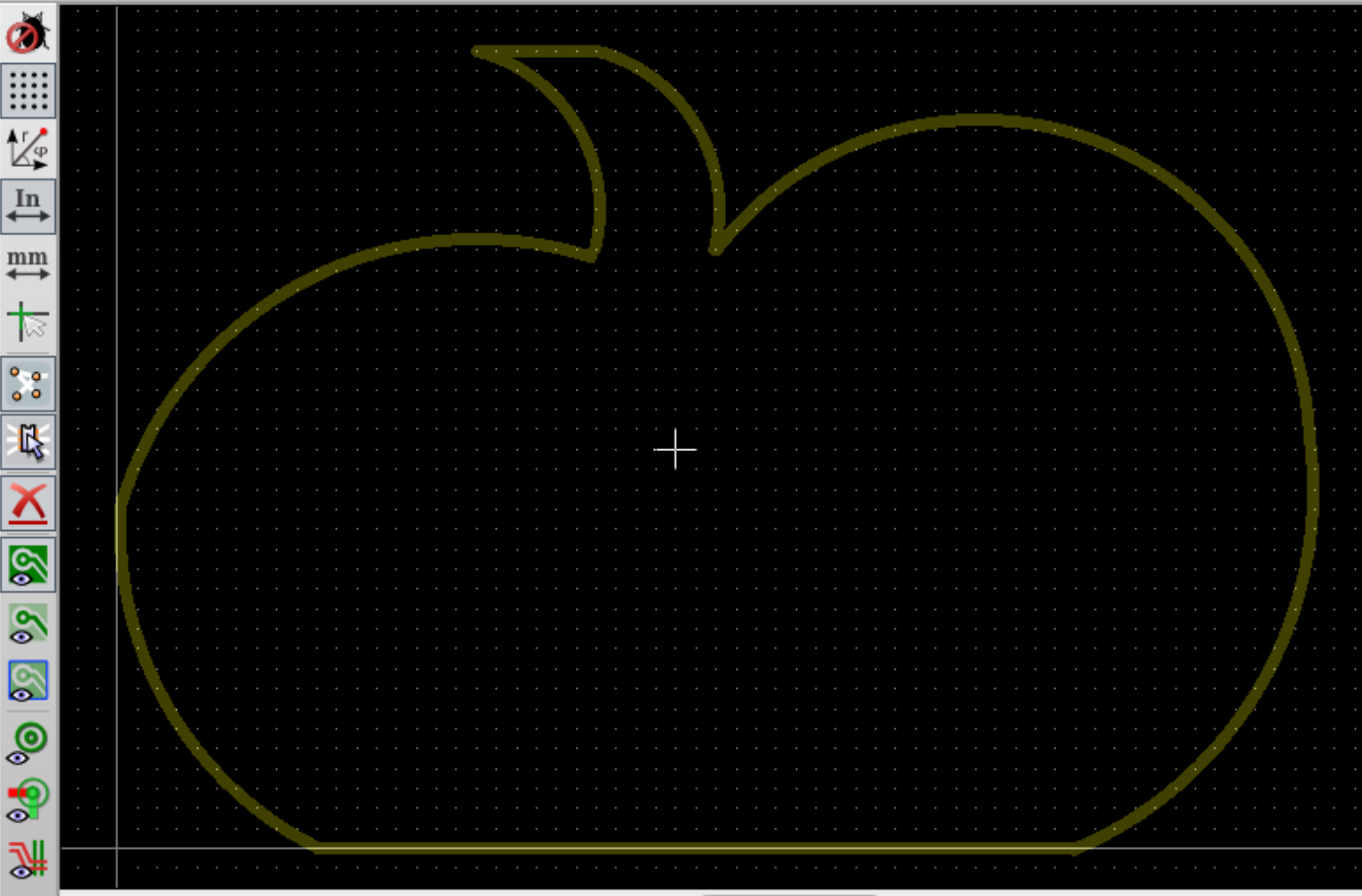
Z 35 X 5.9750 Y 4.5500 dx -1.5150 dy 0.8700 Inches

Create an outline on the PCB_Edges layer





Track 8.0 mils * Via 35.0 mils * Grid 25.0 Zoom 22



Visibles

Layer	Render
Front	<input checked="" type="checkbox"/>
Back	<input checked="" type="checkbox"/>
Adhes_Front	<input checked="" type="checkbox"/>
Adhes_Back	<input checked="" type="checkbox"/>
SoldP_Front	<input checked="" type="checkbox"/>
SoldP_Back	<input checked="" type="checkbox"/>
Silks_Front	<input checked="" type="checkbox"/>
Silks_Back	<input checked="" type="checkbox"/>
Mask_Front	<input checked="" type="checkbox"/>
Mask_Back	<input checked="" type="checkbox"/>
Drawings	<input checked="" type="checkbox"/>
Comments	<input checked="" type="checkbox"/>
Eco1	<input checked="" type="checkbox"/>
Eco2	<input checked="" type="checkbox"/>
PCB_Edges	<input checked="" type="checkbox"/>

Backup file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb3.000
Wrote board file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb3.brd

Grid

The screenshot shows the Pcbnew software interface. The main window displays a PCB design with a green outline on a black grid. A context menu is open over the grid, listing various grid sizes. The 'Grid 2.5' option is highlighted by the mouse cursor. The interface includes a menu bar (File, Edit, View, Place, Preferences, Tools, Design Rules, Help), a toolbar with various icons, and a status bar at the bottom.

Track 8.0 mils * Via 35.0 mils * Grid 25.0 Zoom 22

Grid 100.0
Grid 50.0
Grid 25.0
Grid 20.0
Grid 10.0
Grid 5.0
Grid 2.5
Grid 2.0
Grid 1.0
Grid 0.5
Grid 0.2
Grid 0.1
Grid 196.9
Grid 98.4
Grid 39.4
Grid 19.7
Grid 9.8
Grid 7.9
Grid 3.9
Grid 2.0
Grid 1.0
Grid 0.4
User Grid

Backup file: /home/eric/Dropbox/LowVoltageLabs/Projects/...
Wrote board file: /home/eric/Dropbox/LowVoltageLabs/Proj...
design/the_great_pumpkin_pcb3.000
pcb/design/the_great_pumpkin_pcb3.brd

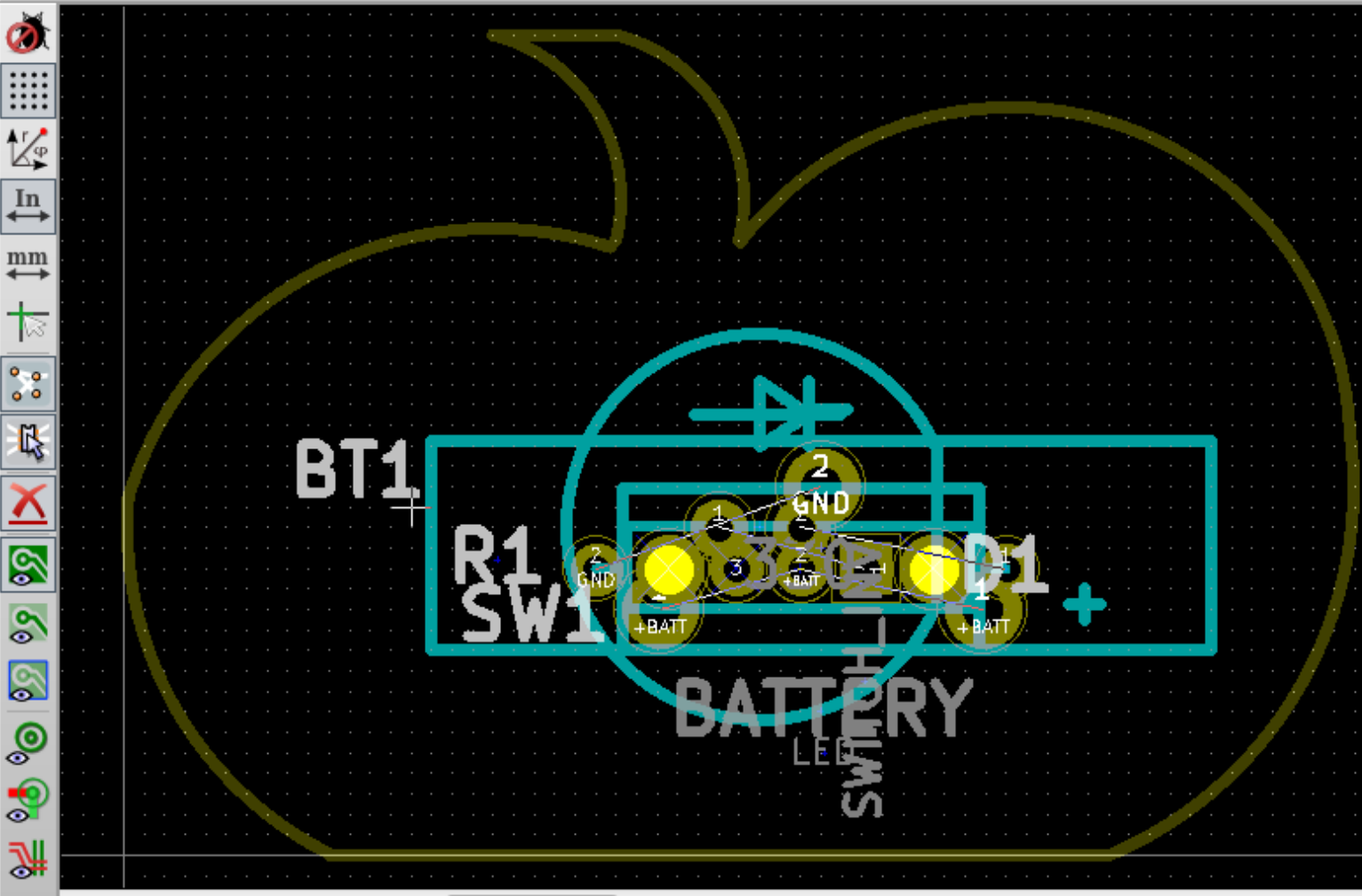
1500 dx 6.7250 dy 3.1500 Inches

Visibles

Layer	Render
Front	<input checked="" type="checkbox"/>
Back	<input checked="" type="checkbox"/>
Adhes_Front	<input checked="" type="checkbox"/>
Adhes_Back	<input checked="" type="checkbox"/>
SoldP_Front	<input checked="" type="checkbox"/>
SoldP_Back	<input checked="" type="checkbox"/>
SilkS_Front	<input checked="" type="checkbox"/>
SilkS_Back	<input checked="" type="checkbox"/>
Mask_Front	<input checked="" type="checkbox"/>
Mask_Back	<input checked="" type="checkbox"/>
Drawings	<input checked="" type="checkbox"/>
Comments	<input checked="" type="checkbox"/>
Eco1	<input checked="" type="checkbox"/>
Eco2	<input checked="" type="checkbox"/>
PCB_Edges	<input checked="" type="checkbox"/>



Track 8.0 mils * Via 35.0 mils * Grid 25.0 Auto



Visibles

Layer	Render
Front	<input checked="" type="checkbox"/>
Back	<input checked="" type="checkbox"/>
Adhes_Front	<input checked="" type="checkbox"/>
Adhes_Back	<input checked="" type="checkbox"/>
SoldP_Front	<input checked="" type="checkbox"/>
SoldP_Back	<input checked="" type="checkbox"/>
Silks_Front	<input checked="" type="checkbox"/>
Silks_Back	<input checked="" type="checkbox"/>
Mask_Front	<input checked="" type="checkbox"/>
Mask_Back	<input checked="" type="checkbox"/>
Drawings	<input checked="" type="checkbox"/>
Comments	<input checked="" type="checkbox"/>
Eco1	<input checked="" type="checkbox"/>
Eco2	<input checked="" type="checkbox"/>
PCB_Edges	<input checked="" type="checkbox"/>

BT1	Last Change	Layer	Pads	Stat	Orient	Module	3D-Shape	Doc: MPD BS-5
BATTERY	Jun 2, 2012	Front	3	.P	0.0	CR2032V_1		KeyW:

Score ??, pos ?? Z 21.4... X 6.3500 Y 3.7750 dx 6.3500 dy 3.7750 Inches

'm' to move parts, ratsnests to help determine locations

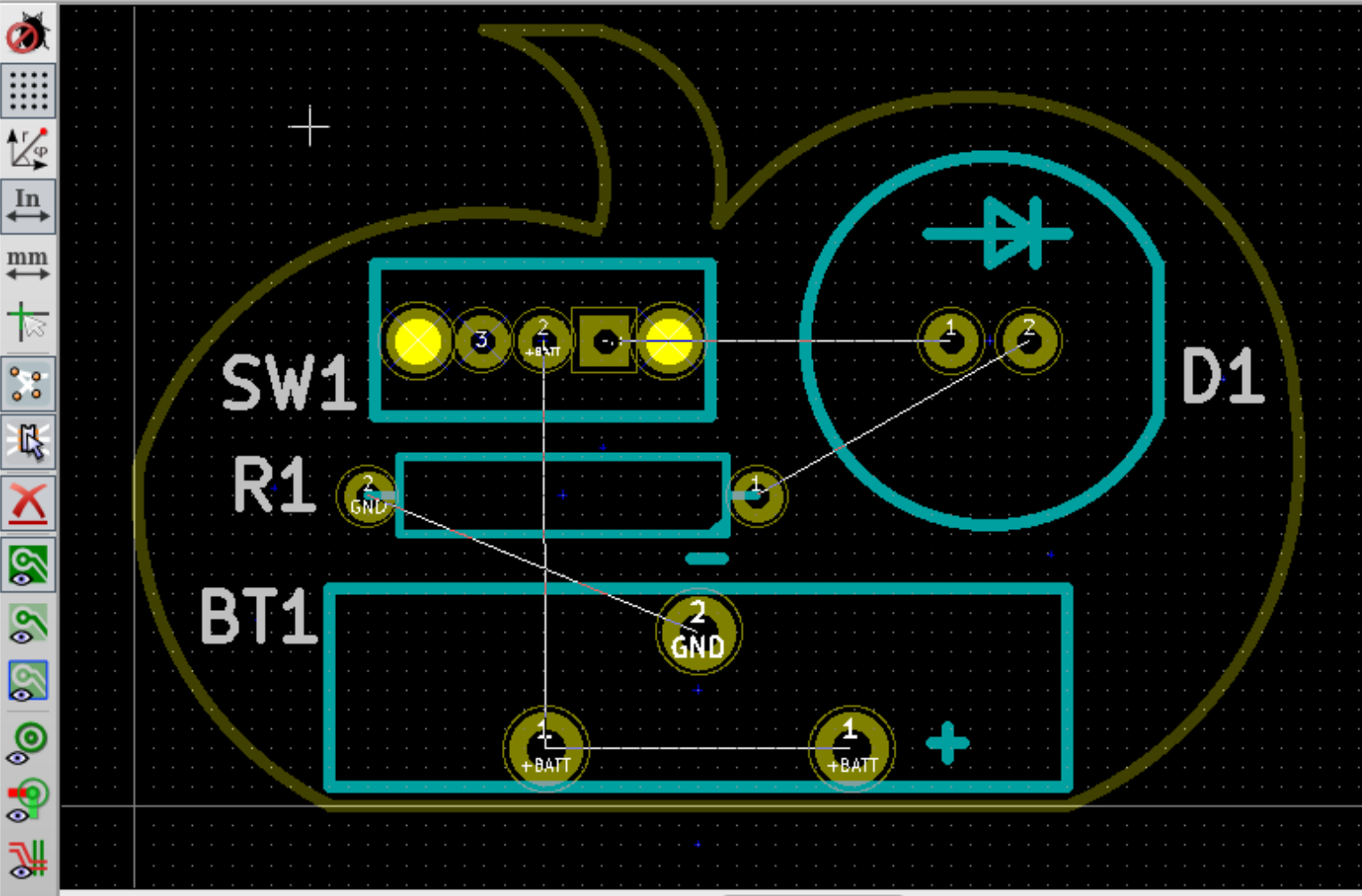
The screenshot displays the Pcbnew software interface for a PCB design project. The main workspace shows a schematic layout of a battery-powered circuit. The components and their connections are as follows:

- BATTERY:** A central component with two positive terminals labeled '+BATT' and one negative terminal labeled 'GND'. It is connected to a resistor (R1) and a switch (SW1).
- R1:** A resistor with a value of 330, connected between the positive terminal of the battery and the negative terminal of the switch.
- SW1:** A switch with two terminals, one connected to the positive terminal of the battery and the other to the positive terminal of an LED.
- LED:** A light-emitting diode with two terminals, one connected to the positive terminal of the switch and the other to the positive terminal of another battery.
- BT1:** A component with two terminals, one connected to the positive terminal of the battery and the other to the positive terminal of the second battery.
- Second Battery:** A smaller battery with two positive terminals labeled '+BATT' and one negative terminal labeled 'GND'. It is connected to the LED and the BT1 component.

The interface includes a menu bar (File, Edit, View, Place, Preferences, Tools, Design Rules, Help), a toolbar with various design tools, and a 'Visibles' panel on the right side. The 'Visibles' panel shows a list of layers and their render status, with most items checked. The status bar at the bottom provides statistics for the design, including Pads (12), Vias (0), trackSegm (0), Nodes (9), Nets (5), Links (5), Connect (0), and Unconnected (5). The current coordinates are Z 21.4..., X 6.9750, Y 3.5000, and the units are set to Inches.



Track 8.0 mils * Via 35.0 mils * Grid 25.0 Auto



Visibles

Layer	Render
<input type="checkbox"/>	<input checked="" type="checkbox"/> Through Via
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> BI/Buried Via
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> Micro Via
<input type="checkbox"/>	<input checked="" type="checkbox"/> Ratsnest
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> Pads Front
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> Pads Back
<input type="checkbox"/>	<input checked="" type="checkbox"/> Text Front
<input type="checkbox"/>	<input checked="" type="checkbox"/> Text Back
<input type="checkbox"/>	<input type="checkbox"/> Hidden Text
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> Anchors
<input type="checkbox"/>	<input checked="" type="checkbox"/> Grid
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> No-Connects
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> Modules Front
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> Modules Back
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> Values
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> References

Backup file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb4.000
Wrote board file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb4.brd

Place a track with shift-x

The screenshot shows the KiCad PCB Editor interface. The main workspace displays a PCB layout with several components and tracks. A red track is being placed, labeled '+BATT'. The track is connected to a component labeled '2'. The track is placed on the 'Front' layer. The status bar at the bottom shows the track details:

Type	NetName	NetCode	Status	Layer	Width	Segment Length	Track Len	Segs Count
Track	+BATT	1.0	..	Front	0.0250 in	0.1750 in	0.1750 "	2

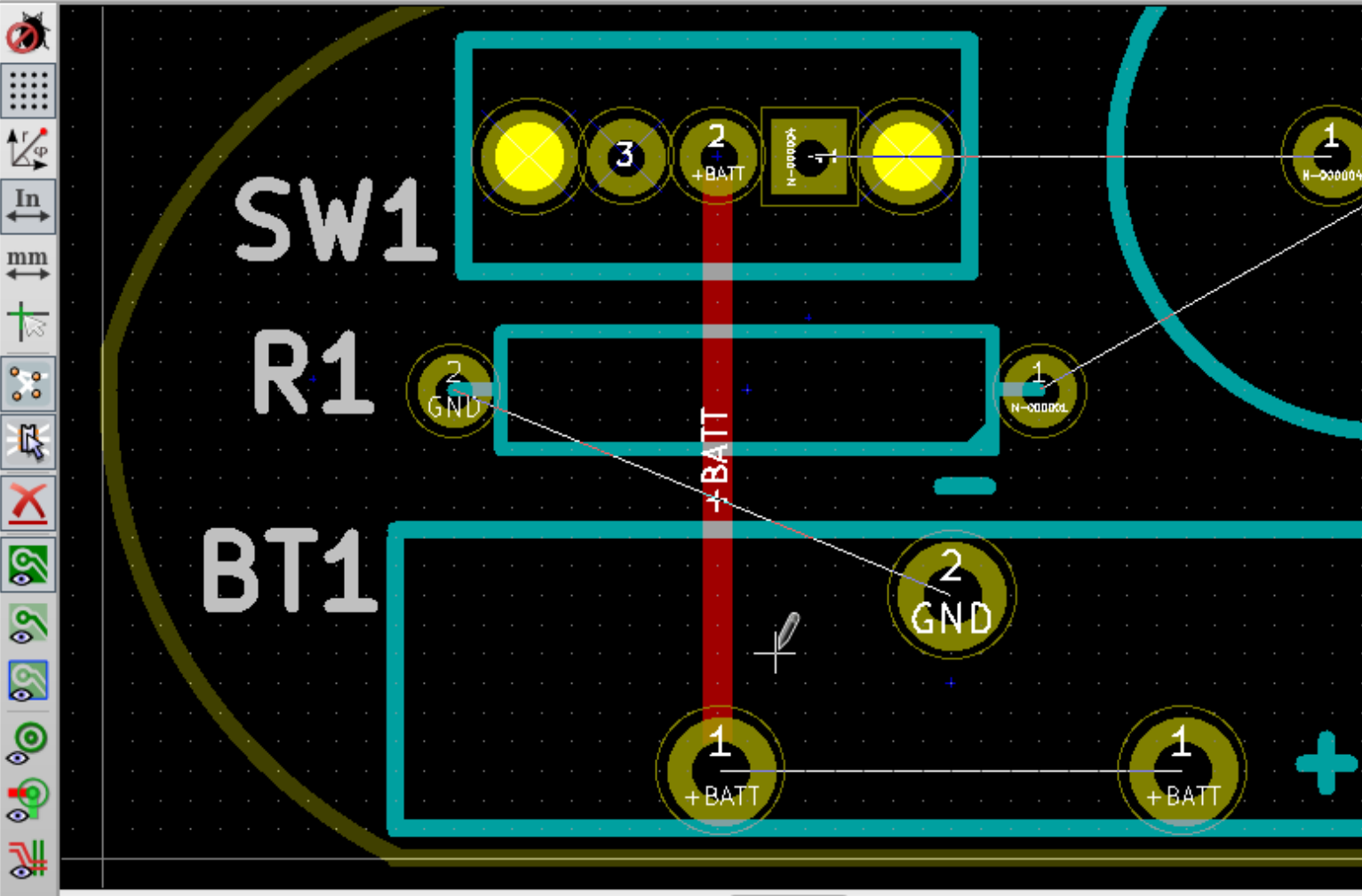
The status bar also shows the track's position and dimensions: links 5 nc 3 net:nc 1, Z 7, X 6.5250 Y 3.7750, dx 6.5250 dy 3.7750. The units are set to Inches, and there is an 'Add tracks' button.

The 'Visibles' panel on the right shows the following layers and their render status:

Layer	Render
Front	<input checked="" type="checkbox"/>
Back	<input checked="" type="checkbox"/>
Adhes_Front	<input checked="" type="checkbox"/>
Adhes_Back	<input checked="" type="checkbox"/>
SoldP_Front	<input checked="" type="checkbox"/>
SoldP_Back	<input checked="" type="checkbox"/>
SilkS_Front	<input checked="" type="checkbox"/>
SilkS_Back	<input checked="" type="checkbox"/>
Mask_Front	<input checked="" type="checkbox"/>
Mask_Back	<input checked="" type="checkbox"/>
Drawings	<input checked="" type="checkbox"/>
Comments	<input checked="" type="checkbox"/>
Eco1	<input checked="" type="checkbox"/>
Eco2	<input checked="" type="checkbox"/>
PCB_Edges	<input checked="" type="checkbox"/>



Track 25.0 mils Via 35.0 mils * Grid 25.0 Zoom 15



Visibles

Layer	Render
Front	<input checked="" type="checkbox"/>
Back	<input checked="" type="checkbox"/>
Adhes_Front	<input checked="" type="checkbox"/>
Adhes_Back	<input checked="" type="checkbox"/>
SoldP_Front	<input checked="" type="checkbox"/>
SoldP_Back	<input checked="" type="checkbox"/>
Silks_Front	<input checked="" type="checkbox"/>
Silks_Back	<input checked="" type="checkbox"/>
Mask_Front	<input checked="" type="checkbox"/>
Mask_Back	<input checked="" type="checkbox"/>
Drawings	<input checked="" type="checkbox"/>
Comments	<input checked="" type="checkbox"/>
Eco1	<input checked="" type="checkbox"/>
Eco2	<input checked="" type="checkbox"/>
PCB_Edges	<input checked="" type="checkbox"/>

Pads	Vias	trackSegm	Nodes	Nets	Links	Connect	Unconnected
12	0	2	9	5	5	1	4

Double click to end the track at the battery

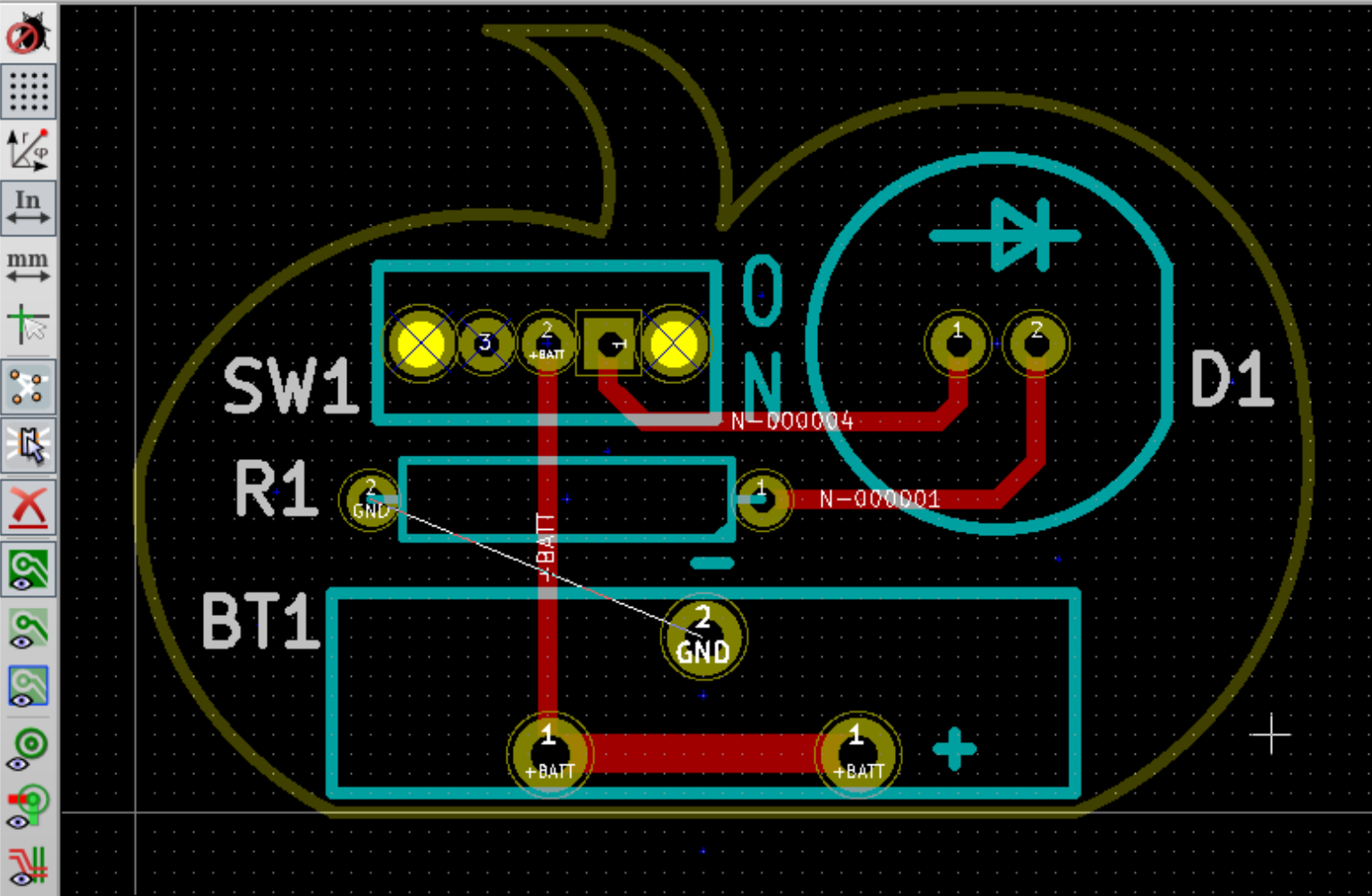
The screenshot shows the Pcbnew software interface. The main workspace displays a PCB layout with a red track being placed. A large white '1' is positioned to the left of the track, and a '2' is positioned to the right of a circular pad labeled 'GND'. A red track is being placed from the pad to a vertical red track labeled '+BATT'. The status bar at the bottom shows design statistics:

Pads	Vias	trackSegm	Nodes	Nets	Links	Connect	Unconnected
12	0	10	9	5	5	3	2

links 5 nc 2 net:nc 1 Z 10 X 6.5280 Y 4.1250 dx 6.5280 dy 4.1250 Inches Add tracks



Track 25.0 mils Via 35.0 mils * Grid 25.0 Auto



Visibles

Layer	Render
Front	<input checked="" type="checkbox"/>
Back	<input checked="" type="checkbox"/>
Adhes_Front	<input checked="" type="checkbox"/>
Adhes_Back	<input checked="" type="checkbox"/>
SoldP_Front	<input checked="" type="checkbox"/>
SoldP_Back	<input checked="" type="checkbox"/>
Silks_Front	<input checked="" type="checkbox"/>
Silks_Back	<input checked="" type="checkbox"/>
Mask_Front	<input checked="" type="checkbox"/>
Mask_Back	<input checked="" type="checkbox"/>
Drawings	<input checked="" type="checkbox"/>
Comments	<input checked="" type="checkbox"/>
Eco1	<input checked="" type="checkbox"/>
Eco2	<input checked="" type="checkbox"/>
PCB_Edges	<input checked="" type="checkbox"/>

Pads	Vias	trackSegm	Nodes	Nets	Links	Connect	Unconnected
12	0	11	9	5	5	4	1

Z 22.5... X 7.4500 Y 4.1000 dx 7.4500 dy 4.1000 Inches Add tracks

Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb4.brd

File Edit View **Place** Preferences Tools Design Rules Help

Track 25.0 mils

Track 25.0 Auto

Module Shift+O
Track Shift+X
Zone
Text
Arc
Circle
Line or Polygon
Dimension
Layer alignment target
Drill and Place Offset
Grid Origin

BT1 D1

N-000004
N-000001
+BATT
GND

Visibles

Layer	Render
Front	<input checked="" type="checkbox"/>
Back	<input checked="" type="checkbox"/>
Adhes_Front	<input checked="" type="checkbox"/>
Adhes_Back	<input checked="" type="checkbox"/>
SoldP_Front	<input checked="" type="checkbox"/>
SoldP_Back	<input checked="" type="checkbox"/>
Silks_Front	<input checked="" type="checkbox"/>
Silks_Back	<input checked="" type="checkbox"/>
Mask_Front	<input checked="" type="checkbox"/>
Mask_Back	<input checked="" type="checkbox"/>
Drawings	<input checked="" type="checkbox"/>
Comments	<input checked="" type="checkbox"/>
Eco1	<input checked="" type="checkbox"/>
Eco2	<input checked="" type="checkbox"/>
PCB_Edges	<input checked="" type="checkbox"/>

Pads	Vias	trackSegm	Nodes	Nets	Links	Connect	Unconnected
12	0	11	9	5	5	4	1

Add filled zones Z 22.5... X 6.5500 Y 3.1750 dx 6.5500 dy 3.1750 Inches

Zone Properties

Layer:

- Front
- Back

Net:

- <no net>
- +BATT
- GND
- N-000001
- N-000004

Net Filtering

Display:

Show all (advanced)

Hidden net filter:

N-*

Visible net filter:

*

Apply Filters

Settings

Clearance ("):

0.0200

Pad connection:

Thermal relief

Fill mode:

Polygon

Outline slope:

Arbitrary

Minimum width ("):

0.0100

Thermal Reliefs

Antipad clearance ("):

0.0200

Segments / 360 deg:

16

Outline style:

Hatched

Corner smoothing:

None

Spoke width ("):

0.0200

0.0000

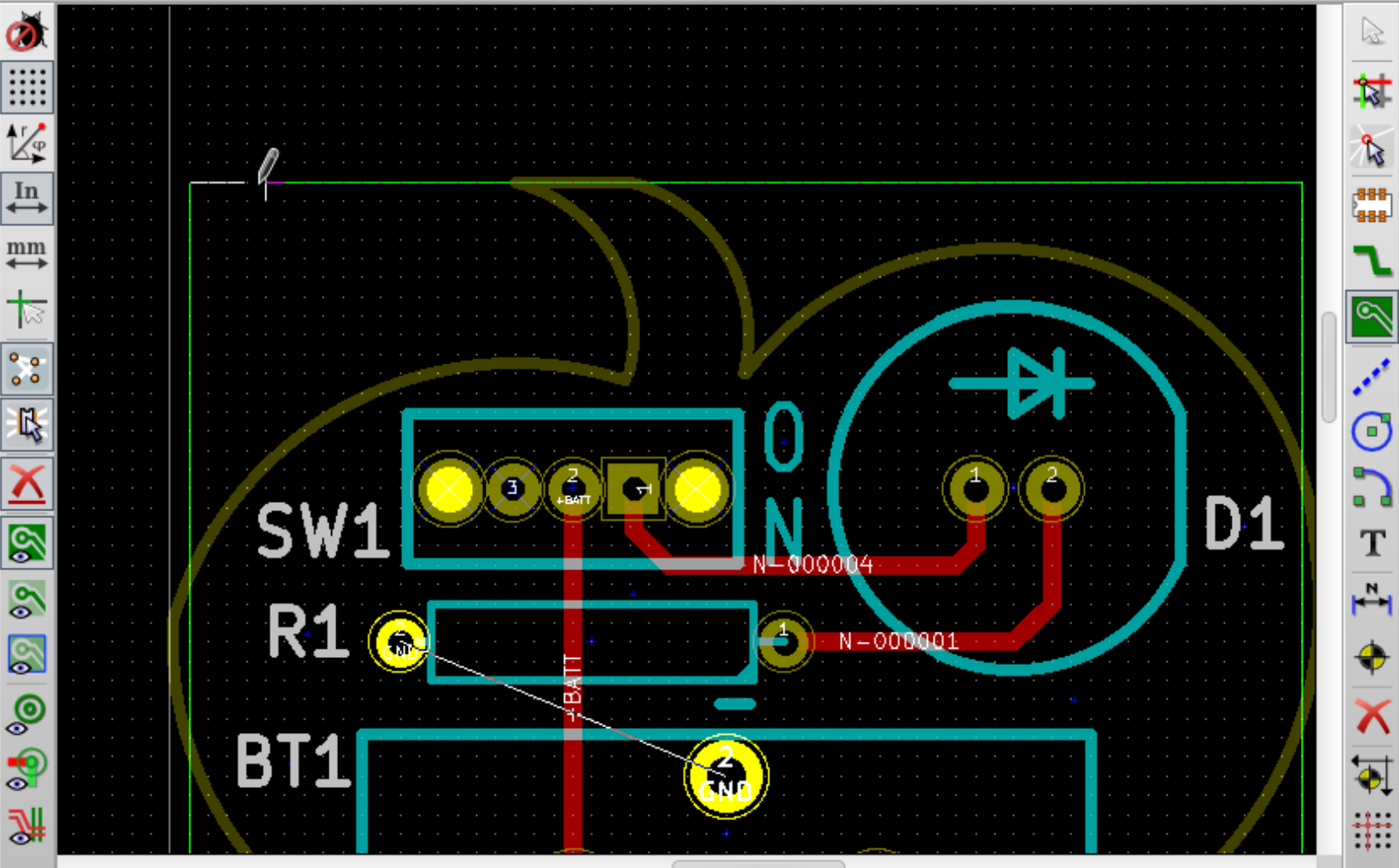
Export Settings to Other Zones

Ok

Cancel



Track 25.0 mils Via 35.0 mils * Grid 25.0 Zoom 22



Visibles

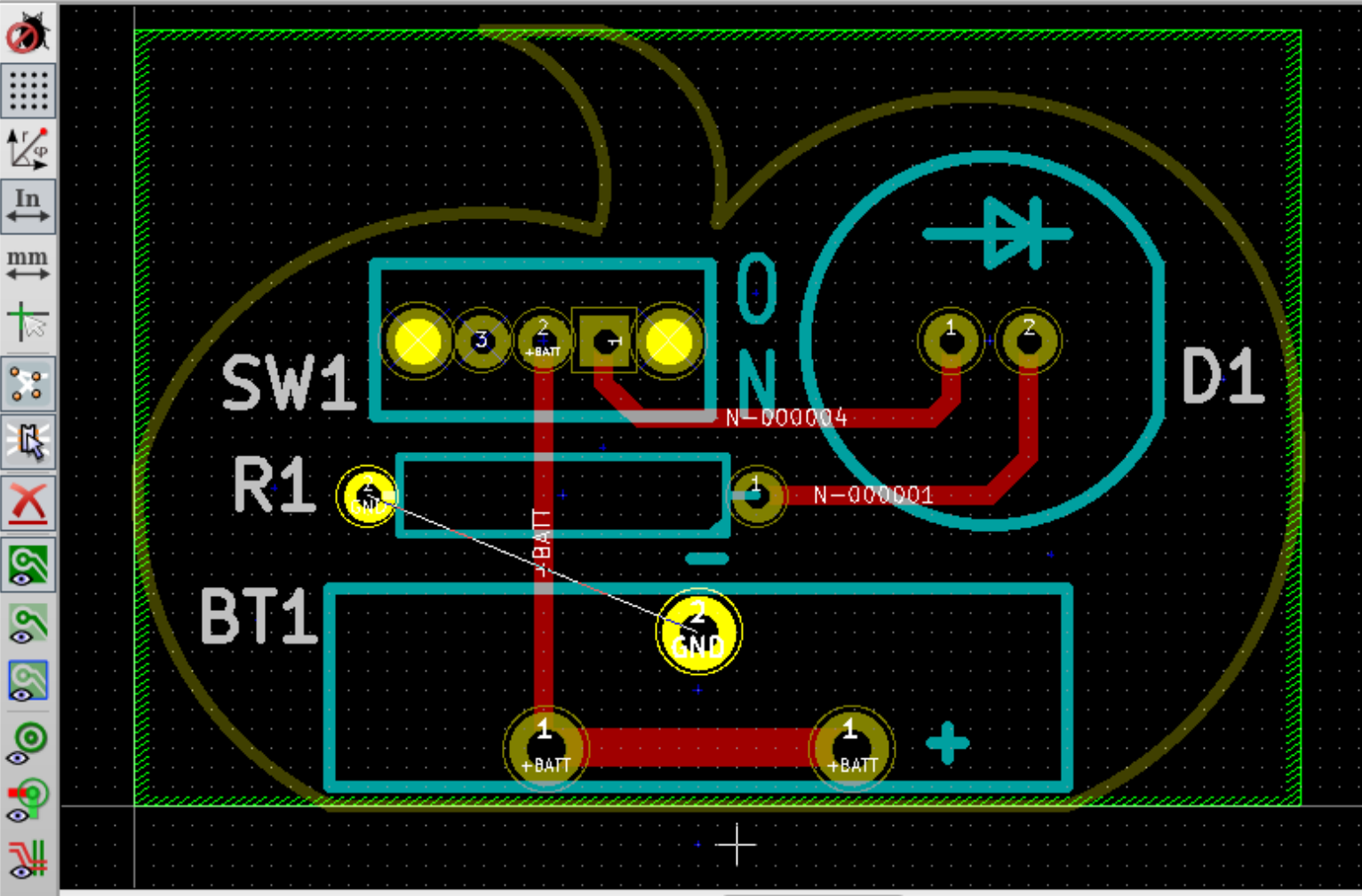
Layer	Render
Front	<input checked="" type="checkbox"/>
Back	<input checked="" type="checkbox"/>
Adhes_Front	<input checked="" type="checkbox"/>
Adhes_Back	<input checked="" type="checkbox"/>
SoldP_Front	<input checked="" type="checkbox"/>
SoldP_Back	<input checked="" type="checkbox"/>
Silks_Front	<input checked="" type="checkbox"/>
Silks_Back	<input checked="" type="checkbox"/>
Mask_Front	<input checked="" type="checkbox"/>
Mask_Back	<input checked="" type="checkbox"/>
Drawings	<input checked="" type="checkbox"/>
Comments	<input checked="" type="checkbox"/>
Eco1	<input checked="" type="checkbox"/>
Eco2	<input checked="" type="checkbox"/>
PCB_Edges	<input checked="" type="checkbox"/>

Type	NetName	NetCode	Layer	Corners	Fill mode	Hatch lines
Zone Outline	GND	2	Back	5	Polygons	0

links 5 nc 2 net:nc 1 Z 22 X 6.1250 Y 3.2000 dx 6.1250 dy 3.2000 Inches Add zones



Track 25.0 mils Via 35.0 mils * Grid 25.0 Auto



Visibles

Layer	Render
Front	<input checked="" type="checkbox"/>
Back	<input checked="" type="checkbox"/>
Adhes_Front	<input checked="" type="checkbox"/>
Adhes_Back	<input checked="" type="checkbox"/>
SoldP_Front	<input checked="" type="checkbox"/>
SoldP_Back	<input checked="" type="checkbox"/>
Silks_Front	<input checked="" type="checkbox"/>
Silks_Back	<input checked="" type="checkbox"/>
Mask_Front	<input checked="" type="checkbox"/>
Mask_Back	<input checked="" type="checkbox"/>
Drawings	<input checked="" type="checkbox"/>
Comments	<input checked="" type="checkbox"/>
Eco1	<input checked="" type="checkbox"/>
Eco2	<input checked="" type="checkbox"/>
PCB_Edges	<input checked="" type="checkbox"/>

Pads	Vias	trackSegm	Nodes	Nets	Links	Connect	Unconnected
12	0	11	9	5	5	4	1

Z 22.5... X 6.7750 Y 4.2500 dx 6.7750 dy 4.2500 Inches Add zones

Right click on the zone

The screenshot shows a PCB design software interface with a right-click context menu open over a green zone. The menu options are:

- Zones
- Get and Move Footprint (T)
- Select Working Layer
- Center (F4)
- Zoom in (F1)
- Zoom out (F2)
- Redraw view (F3)
- Zoom auto (Home)
- Zoom select
- Grid Select
- Close

The secondary context menu options are:

- Create Corner
- Drag Outline Segment (G)
- Add Similar Zone
- Add Cutout Area
- Fill Zone (highlighted by the mouse)
- Move Zone (M)
- Edit Zone Params (E)
- Delete Zone Outline

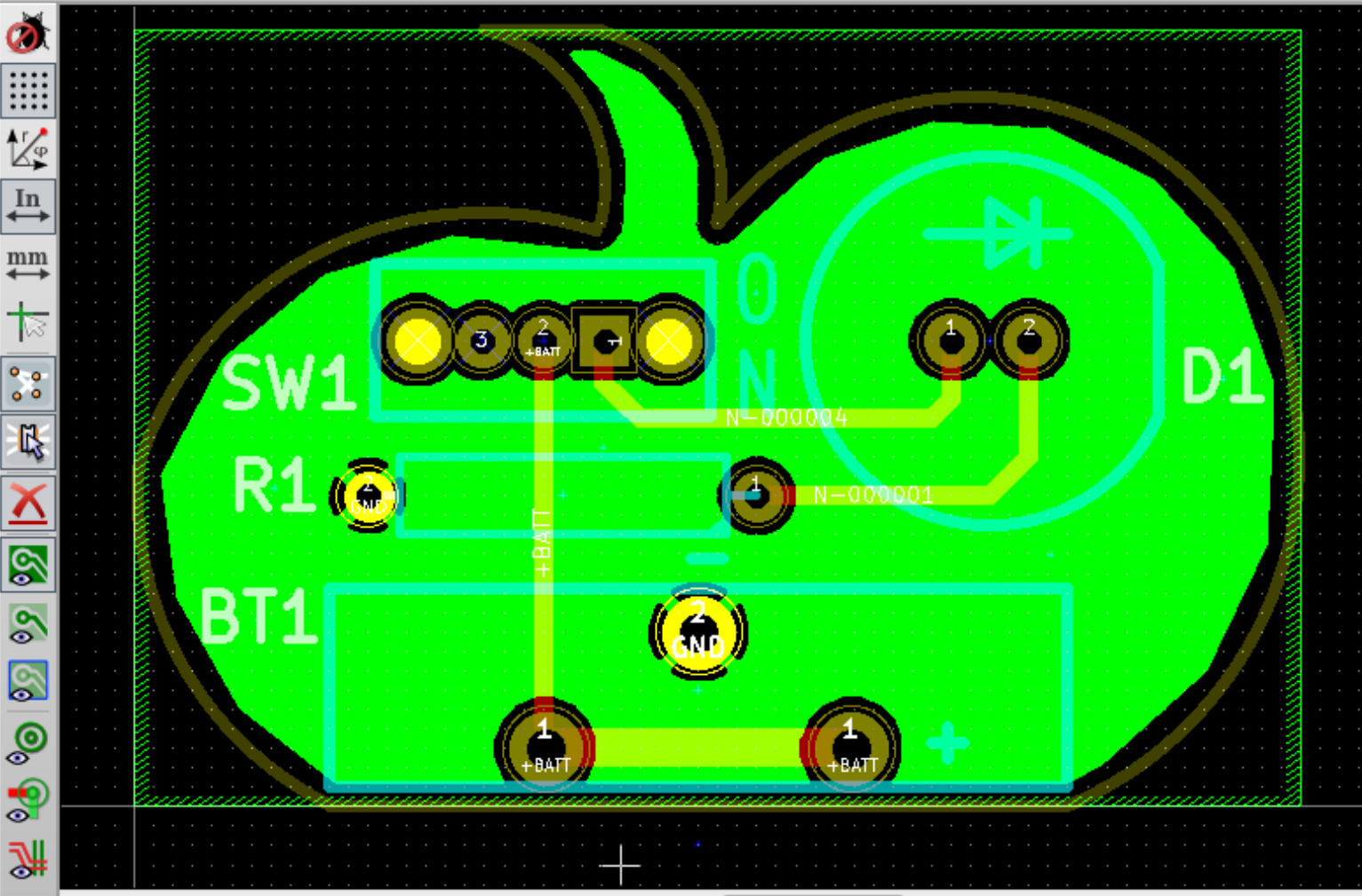
The PCB design shows a green zone with a red track and a yellow circular pad labeled "1 +BATT". A large white "D1" label is visible on the right. The status bar at the bottom displays the following information:

Type	NetName	NetCode	Layer	Corners	Fill mode	Hatch lines
Zone Outline	GND	2	Back	4	Polygons	406

Additional status bar information includes: Z 22.5..., X 6.0000 Y 3.3500, dx 6.0000 dy 3.3500, and Inches.



Track 25.0 mils Via 35.0 mils * Grid 25.0 Auto



Visibles

Layer	Render
Front	<input checked="" type="checkbox"/>
Back	<input checked="" type="checkbox"/>
Adhes_Front	<input checked="" type="checkbox"/>
Adhes_Back	<input checked="" type="checkbox"/>
SoldP_Front	<input checked="" type="checkbox"/>
SoldP_Back	<input checked="" type="checkbox"/>
Silks_Front	<input checked="" type="checkbox"/>
Silks_Back	<input checked="" type="checkbox"/>
Mask_Front	<input checked="" type="checkbox"/>
Mask_Back	<input checked="" type="checkbox"/>
Drawings	<input checked="" type="checkbox"/>
Comments	<input checked="" type="checkbox"/>
Eco1	<input checked="" type="checkbox"/>
Eco2	<input checked="" type="checkbox"/>
PCB_Edges	<input checked="" type="checkbox"/>

Pads	Vias	trackSegm	Nodes	Nets	Links	Connect	Unconnected
12	0	11	9	5	5	5	0

Place text on the board

The screenshot shows the Pcbnew software interface. The 'Place' menu is open, and the 'Text' option is selected. The 'Text Properties' dialog box is displayed, showing the text 'Seattle Mini Maker Faire 2012' and various settings for size, position, orientation, and layer. The PCB layout shows a green copper layer with a white text label 'R1' and a circular pad labeled '2 GND'.

Text Properties

Text:
Seattle Mini
Maker Faire
2012

Size X ("): 0.0500
Position X ("): 7.2250
Orientation: 0
Display: Mirrored

Size Y ("): 0.0500
Position Y ("): 3.7000
Style: Normal
Justification: Center

Thickness ("): 0.0100
Layer: Back

Cancel OK

Track 8.0 mils *
d 25.0 Zoom 10

File Edit View Place Preferences Tools Design Rules Help

Module Shift+O
Track Shift+X
Zone
Text
Arc
Circle
Line or Polygon
Dimension
Layer alignment target
Drill and Place Offset
Grid Origin

Visibles
Layer Render
Through Via
BI/Buried Via
Micro Via
Ratsnest

Pads 12 Vias 0 trackSegm 11 Nodes 9 Nets 5 Links 5

Add text on copper layers or graphic text Z 10

Back copper layer

Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.brd

File Edit View Place Preferences Tools Design Rules Help

Track 8.0 mils * Via 35.0 mils * Grid 25.0 Zoom 10

Back (Alt+4)

Visibles

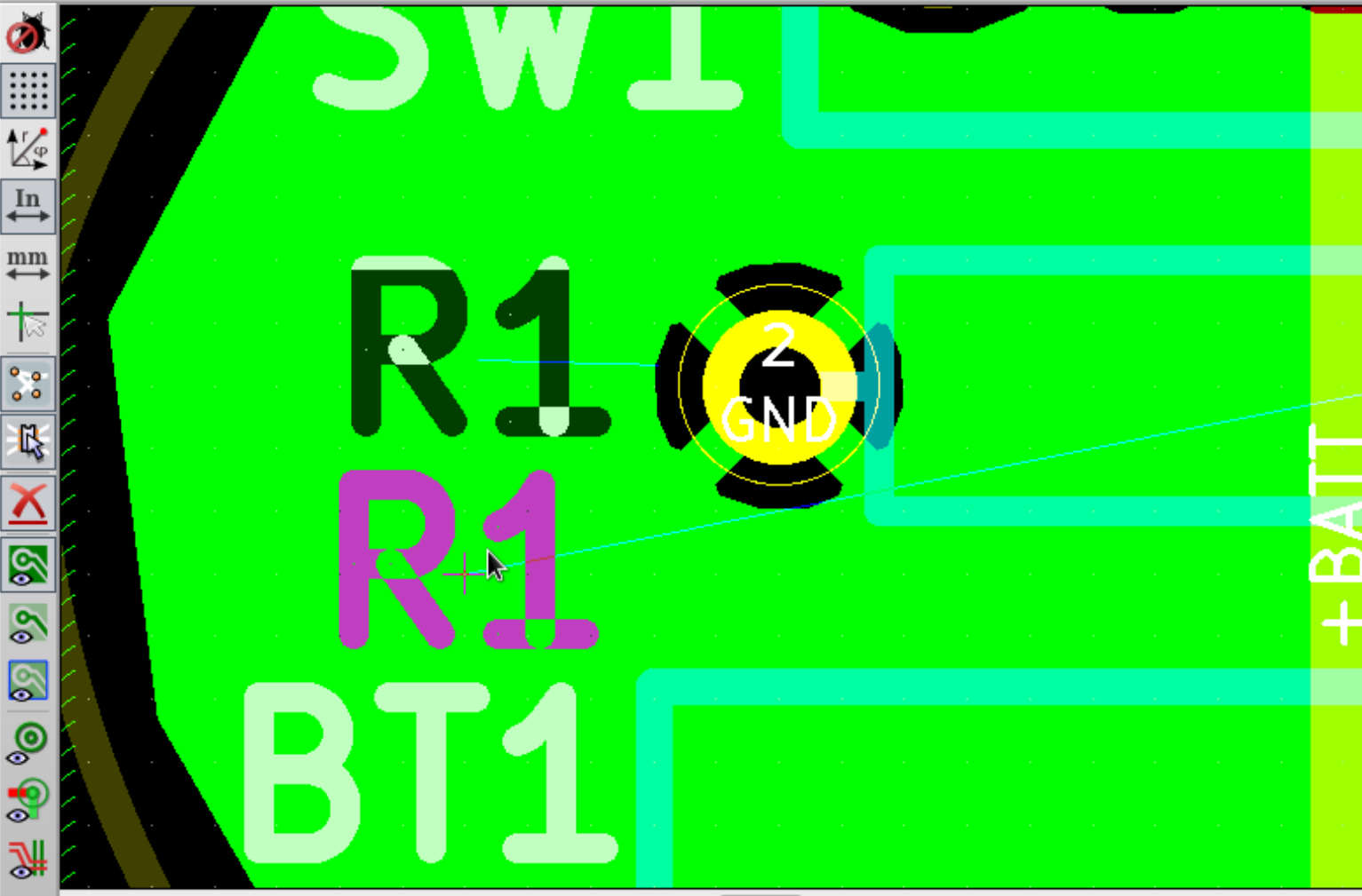
Layer	Render
Front	<input checked="" type="checkbox"/>
Back	<input checked="" type="checkbox"/>
Adhes_Front	<input checked="" type="checkbox"/>
Adhes_Back	<input checked="" type="checkbox"/>
SoldP_Front	<input checked="" type="checkbox"/>
SoldP_Back	<input checked="" type="checkbox"/>
SilkS_Front	<input checked="" type="checkbox"/>
SilkS_Back	<input checked="" type="checkbox"/>
Mask_Front	<input checked="" type="checkbox"/>
Mask_Back	<input checked="" type="checkbox"/>
Drawings	<input checked="" type="checkbox"/>
Comments	<input checked="" type="checkbox"/>
Eco1	<input checked="" type="checkbox"/>
Eco2	<input checked="" type="checkbox"/>
PCB_Edges	<input checked="" type="checkbox"/>

Pads	Vias	trackSegm	Nodes	Nets	Links	Connect	Unconnected
12	0	11	9	5	5	5	0

Z 10 X 7.4500 Y 3.8750 dx 7.4500 dy 3.8750 Inches



Track 25.0 mils Via 35.0 mils * Grid 25.0 Zoom 7



Visibles

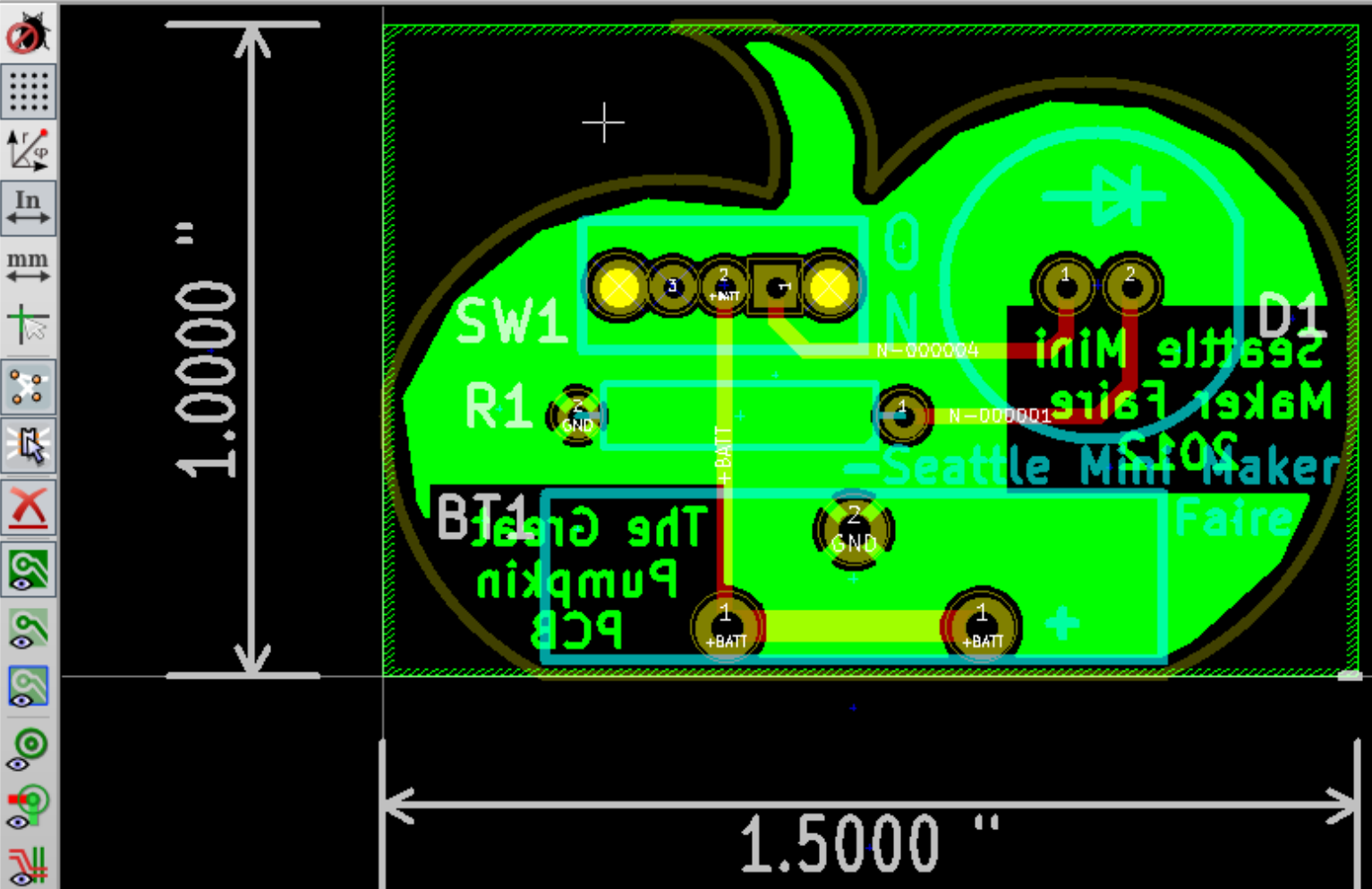
Layer	Render
Front	<input checked="" type="checkbox"/>
Back	<input checked="" type="checkbox"/>
Adhes_Front	<input checked="" type="checkbox"/>
Adhes_Back	<input checked="" type="checkbox"/>
SoldP_Front	<input checked="" type="checkbox"/>
SoldP_Back	<input checked="" type="checkbox"/>
Silks_Front	<input checked="" type="checkbox"/>
Silks_Back	<input checked="" type="checkbox"/>
Mask_Front	<input checked="" type="checkbox"/>
Mask_Back	<input checked="" type="checkbox"/>
Drawings	<input checked="" type="checkbox"/>
Comments	<input checked="" type="checkbox"/>
Eco1	<input checked="" type="checkbox"/>
Eco2	<input checked="" type="checkbox"/>
PCB_Edges	<input checked="" type="checkbox"/>

Module	Text	Type	Display	Layer	Mirror	Orient	Thickness	H Size	V Size
R1	R1	Ref.	Yes	Silks_Front	No	0.0	0.0120 "	0.0600 "	0.0600 "

links 5 nc 0 net:nc 0 Z 7 X 6.1750 Y 3.8750 dx 6.1750 dy 3.8750 Inches



Track 8.0 mils * Via 35.0 mils * Grid 10.0 Auto



Visibles

Layer	Render
Front	<input checked="" type="checkbox"/>
Back	<input checked="" type="checkbox"/>
Adhes_Front	<input checked="" type="checkbox"/>
Adhes_Back	<input checked="" type="checkbox"/>
SoldP_Front	<input checked="" type="checkbox"/>
SoldP_Back	<input checked="" type="checkbox"/>
Silks_Front	<input checked="" type="checkbox"/>
Silks_Back	<input checked="" type="checkbox"/>
Mask_Front	<input checked="" type="checkbox"/>
Mask_Back	<input checked="" type="checkbox"/>
Drawings	<input checked="" type="checkbox"/>
Comments	<input checked="" type="checkbox"/>
Eco1	<input checked="" type="checkbox"/>
Eco2	<input checked="" type="checkbox"/>
PCB_Edges	<input checked="" type="checkbox"/>

Backup file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.000
Wrote board file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.brd

Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/Lo

File Edit **View** Place Preferences Tools Design Rules

Track 8.0 mil

Zoom In Alt+F1

Zoom Out Alt+F2

Fit on Screen

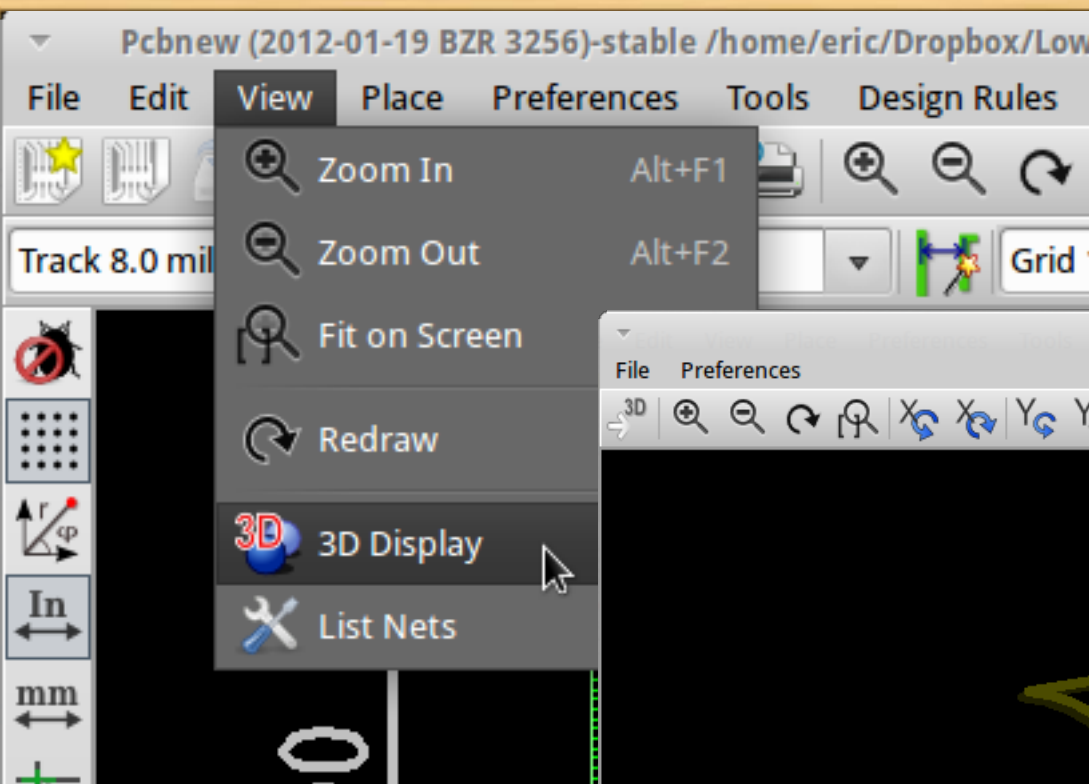
Redraw

3D 3D Display

List Nets

In

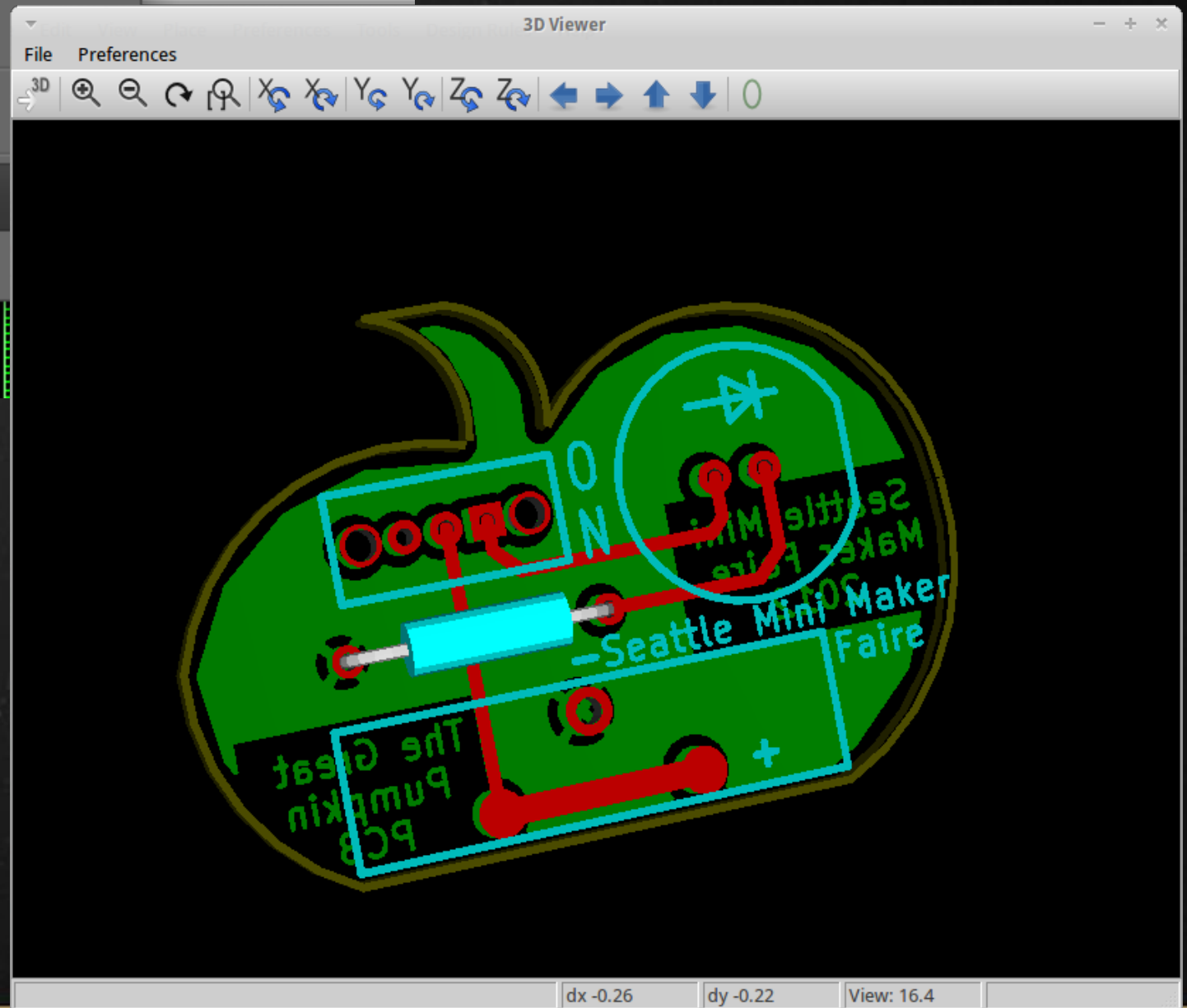
mm



3D Viewer

File Preferences

3D



dx -0.26 dy -0.22 View: 16.4



Create a board with KiCAD

- What is a PCB?
- What is a KiCAD?
- Block diagram
- Schematic
- Schematic attribute editor
- Error check the schematic
- PCB layout
- **Error check the layout**
- Gerber files
- Build boards

Pcbnew (2012-01-19 BZR 3256)-stable /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.brd

File Edit View Place Preferences Tools Design Rules Help

Track 8.0 mils * Via 35.0 mils * 10.0 Auto

Netlist
Layer Pair
DRC
FreeRoute

1.0000 " 1.5000 "

SW1 R1 BT1 D1

Seattle Mini Maker Faire

Backup file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.000
Wrote board file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.brd

Perform design rules check Z 27.2... X 6.4100 Y 3.1600 dx 6.4100 dy 3.1600 Inches

Check for unconnected pads

DRC Control [X]

Options:

Clearance:

Min track width (""):

Min via size (""):

Min uVia size (""):

Create Report File

...

Messages:

Start DRC

List Unconnected

Delete All Markers

Delete Current Marker

Error Messages:

Problems / Markers | Unconnected

ErrType(2): **Unconnected pads**

- Pad [1] (all copper layers) of D1

Cancel OK

DRC Control

Options:

Clearance

Min track width ("):

Min via size ("):

Min uVia size ("):

Create Report File

Messages:

Compile ratsnest...
Pad clearances...
Track clearances...
Fill zones...
Test zones...
Unconnected pads...
Finished

Error Messages:

Create a board with KiCAD

- What is a PCB?
- What is a KiCAD?
- Block diagram
- Schematic
- Schematic attribute editor
- Error check the schematic
- PCB layout
- Error check the layout
- **Gerber files**
- Build boards

File -> Plot to generate gerber files

The screenshot shows the Pcbnew software interface. The 'File' menu is open, and the 'Plot' option is highlighted. The main workspace displays a PCB layout for a pumpkin-shaped board. The board is green with various components and traces. A dimension line at the bottom indicates a width of 1.5000 inches. The status bar at the bottom shows the plot settings: 'Plot board in HPGL, PostScript or Gerber RS-274X format) | Z 27.2... | X 5.7500 Y 3.1900 | dx 5.7500 dy 3.1900 | Inches'.

Backup file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.000
Wrote board file: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/the_great_pumpkin_pcb.brd

Layer	Render
Front	<input checked="" type="checkbox"/>
Back	<input checked="" type="checkbox"/>
Adhes_Front	<input checked="" type="checkbox"/>
Adhes_Back	<input checked="" type="checkbox"/>
SoldP_Front	<input checked="" type="checkbox"/>
SoldP_Back	<input checked="" type="checkbox"/>
SilkS_Front	<input checked="" type="checkbox"/>
SilkS_Back	<input checked="" type="checkbox"/>
Mask_Front	<input checked="" type="checkbox"/>
Mask_Back	<input checked="" type="checkbox"/>
Drawings	<input checked="" type="checkbox"/>
Comments	<input checked="" type="checkbox"/>
Eco1	<input checked="" type="checkbox"/>
Eco2	<input checked="" type="checkbox"/>
PCB_Edges	<input checked="" type="checkbox"/>

Plot

Plot format:

Gerber

Output directory:

gerbers/

Browse...

Layers

- Back
- Adhes_Front
- Adhes_Back
- SoldP_Front
- SoldP_Back
- SilkS_Front
- SilkS_Back
- Mask_Front
- Mask_Back
- Drawings
- Comments
- Eco1
- Eco2
- PCB_Edges

Options

- Plot sheet reference on all layers
- Plot pads on silkscreen
- Plot module value on silkscreen
- Plot module reference on silkscreen
- Plot other module texts on silkscreen
- Plot invisible texts on silkscreen
- Do not tent vias
- Mirrored plot

Drill marks:

Small

Scaling:

1:1

Plot mode:

Filled

Default linewidth ("):

0.0060

Gerber Options

- Use proper filename extensions
- Exclude PCB edge layer from other layers
- Subtract soldermask from silkscreen
- Use auxiliary axis as origin

Messages:

```
gerbers/the_great_pumpkin_pcb-Drawings.gbr> created
Plot file </home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/
gerbers/the_great_pumpkin_pcb-PCB_Edges.gbr> created
```

Plot

Generate Drill File

Close

Plot

Plot format:

Gerber

Output directory:

gerbers/

Browse...

Drill Files Generation

Drill Units:

- Millimeters
- Inches

Zeros Format

- Decimal format
- Suppress leading zeros
- Suppress trailing zeros
- Keep zeros

Precision

- 2:3
- 2:4

Drill Origin:

- Absolute
- Auxiliary axis

Drill Sheet:

- None
- Drill map (HPGL)
- Drill map (PostScript)
- Drill map (Gerber)
- Drill map (DXF)

Drill Report:

- None
- Drill report

HPGL plotter Options:

Speed (cm/s)

20

Pen Number

1

Options:

- Mirror y axis
- Minimal header

Info:

Default Vias Drill:

Use Netclasses values

Micro Vias Drill:

Use Netclasses values

Holes Count:

Plated Pads: 10

Not Plated Pads: 2

Through Vias: 0

Micro Vias: 0

Buried Vias: 0

OK

Cancel

Plot

Generate Drill File

Close



- the_great_pumpkin_pcb.pro
- the_great_pumpkin_pcb.brd
- the_great_pumpkin_pcb.net
- the_great_pumpkin_pcb.sch



Working dir: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design
Project: the_great_pumpkin_pcb.pro

GerbView (Gerber viewer)



Layer 1

No tool

Layer 1 not in use



Visibles

Layer	Render
<input checked="" type="checkbox"/> Layer 1	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 2	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 3	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 4	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 5	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 6	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 7	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 8	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 9	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 10	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 11	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 12	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 13	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 14	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 15	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 16	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 17	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 18	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 19	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 20	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 21	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 22	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 23	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 24	<input checked="" type="checkbox"/>

- GERBER Load Gerber File
- Load EXCELLON Drill File
- GERBER Load DCodes
- Open Recent Gerber File
- Open Recent Drill File
- Clear All
- Export to Pcbnew
- Print
- Exit Ctrl+Q

Layer 1

No tool

Layer 1 not in use

Visibles

Layer	Render
<input checked="" type="checkbox"/> Layer 1	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 2	<input checked="" type="checkbox"/>
<input type="checkbox"/> Layer 3	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 4	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 5	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 6	<input checked="" type="checkbox"/>
<input type="checkbox"/> Layer 7	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 8	<input checked="" type="checkbox"/>
<input type="checkbox"/> Layer 9	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 10	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 11	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 12	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 13	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 14	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 15	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 16	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 17	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 18	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 19	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 20	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 21	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 22	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 23	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 24	<input checked="" type="checkbox"/>

Open Gerber File



eric

Dropbox

LowVoltageLabs

Projects

the_great_pumpkin_pcb

design

gerbers

Places

Search

Recently Used

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27 GB Filesystem

Lenovo_Recovery

Windows7_OS

SYSTEM_DRV

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Music

Pictures

Videos

Clients

Name



Size

Modified

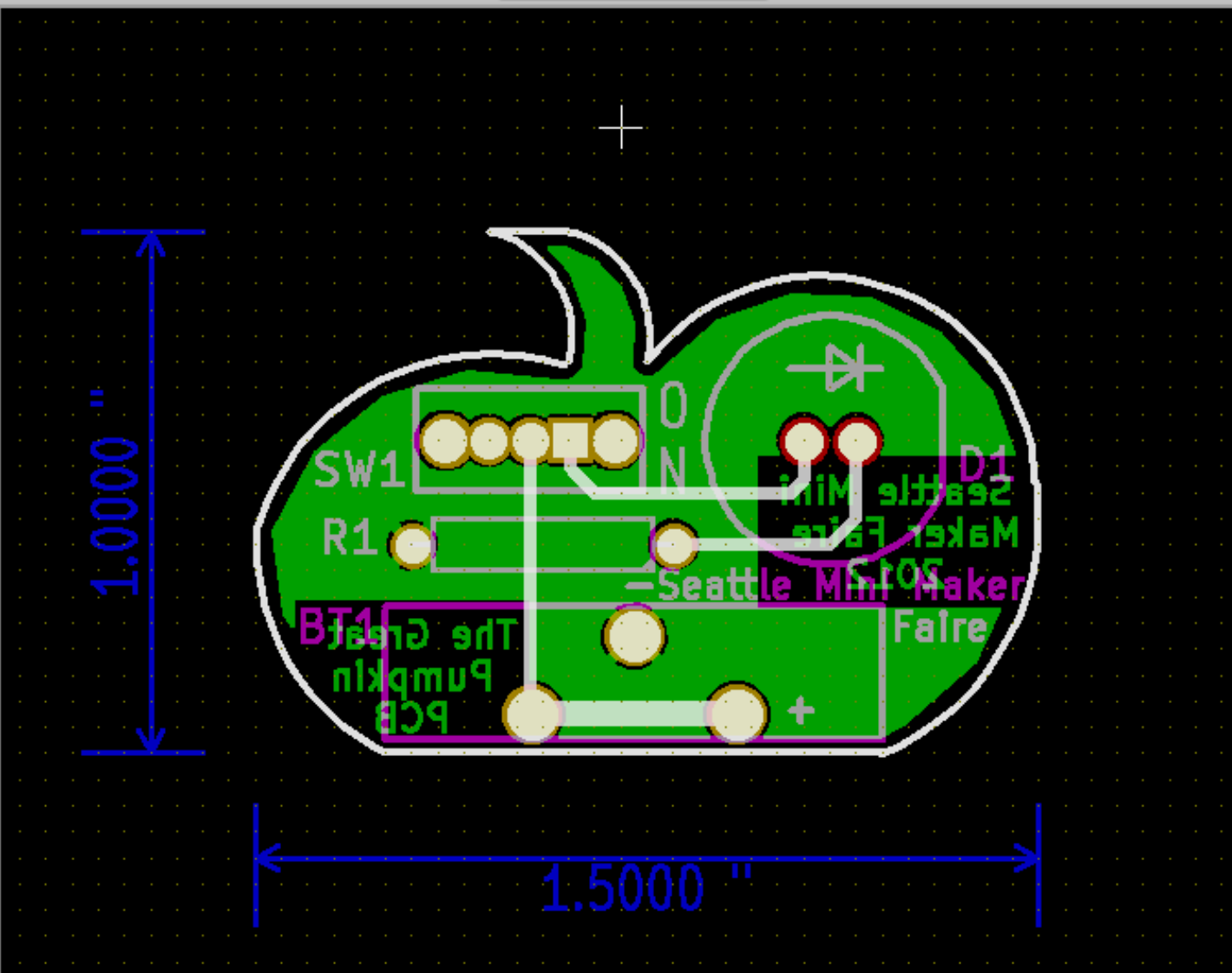
the_great_pumpkin_pcb-Back.gbl	20.4 KB	13:12
the_great_pumpkin_pcb-Drawings.gbr	6.4 KB	13:12
the_great_pumpkin_pcb-Front.gtl	3.3 KB	13:12
the_great_pumpkin_pcb-Mask_Back.gbs	2.8 KB	13:12
the_great_pumpkin_pcb-Mask_Front.gts	2.8 KB	13:12
the_great_pumpkin_pcb-PCB_Edges.gbr	2.4 KB	13:12
the_great_pumpkin_pcb-Silks_Back.gbo	2.4 KB	13:12
the_great_pumpkin_pcb-Silks_Front.gto	10.6 KB	13:12



Gerber files (.g* .lgr .pho)

Cancel

Open

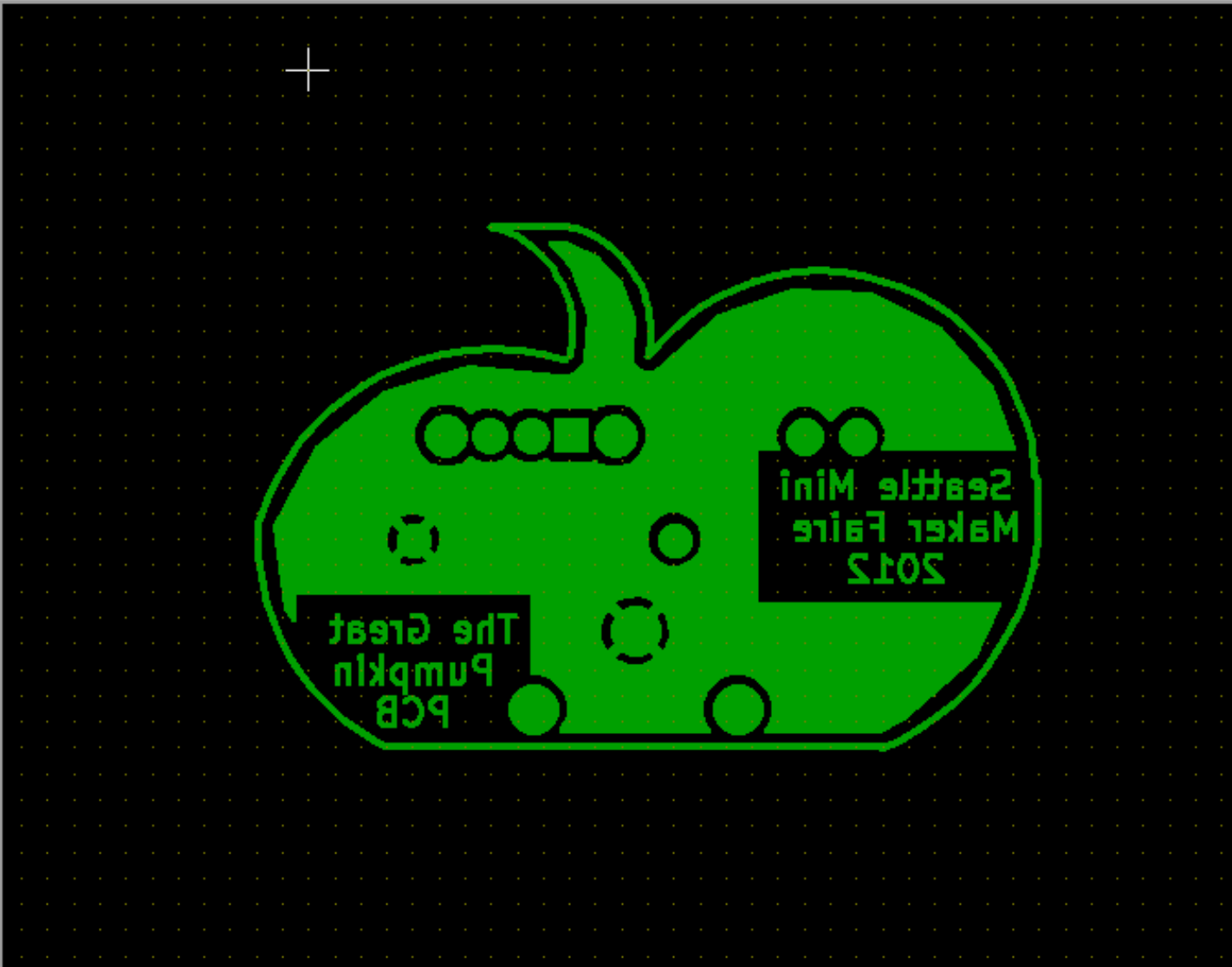


Visibles

Layer	Render
<input type="checkbox"/> Layer 1	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 2	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 3	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 4	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 5	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 6	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 7	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 8	<input checked="" type="checkbox"/>
<input type="checkbox"/> Layer 9	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 10	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 11	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 12	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 13	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 14	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 15	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 16	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 17	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 18	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 19	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 20	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 21	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 22	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 23	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 24	<input checked="" type="checkbox"/>

Image name	Graphic layer	Img Rot.	Polarity	X Justify	Y Justify	Image Justify Offset
no name	1	0	Normal	Normal	Normal	X=0.000000 Y=0.000000

Image name: "no name" Layer name: "no n..." Z 35 X 6.7000 Y 3.0000 dx 6.7000 dy 3.0000 Inches



Visibles

- Layer Render
- Layer 1
- Layer 2
- Layer 3
- Layer 4
- Layer 5
- Layer 6
- Layer 7
- Layer 8
- Layer 9
- Layer 10
- Layer 11
- Layer 12
- Layer 13
- Layer 14
- Layer 15
- Layer 16
- Layer 17
- Layer 18
- Layer 19
- Layer 20
- Layer 21
- Layer 22
- Layer 23
- Layer 24

Image name	Graphic layer	Img Rot.	Polarity	X Justify	Y Justify	Image Justify Offset
no name	1	0	Normal	Normal	Normal	X=0.000000 Y=0.000000

File: /home/eric/Dropbox/LowVoltageLabs/Projects/the_great_pumpkin_pcb/design/gerbers/the_great_pumpkin_pcb-Back.gbl

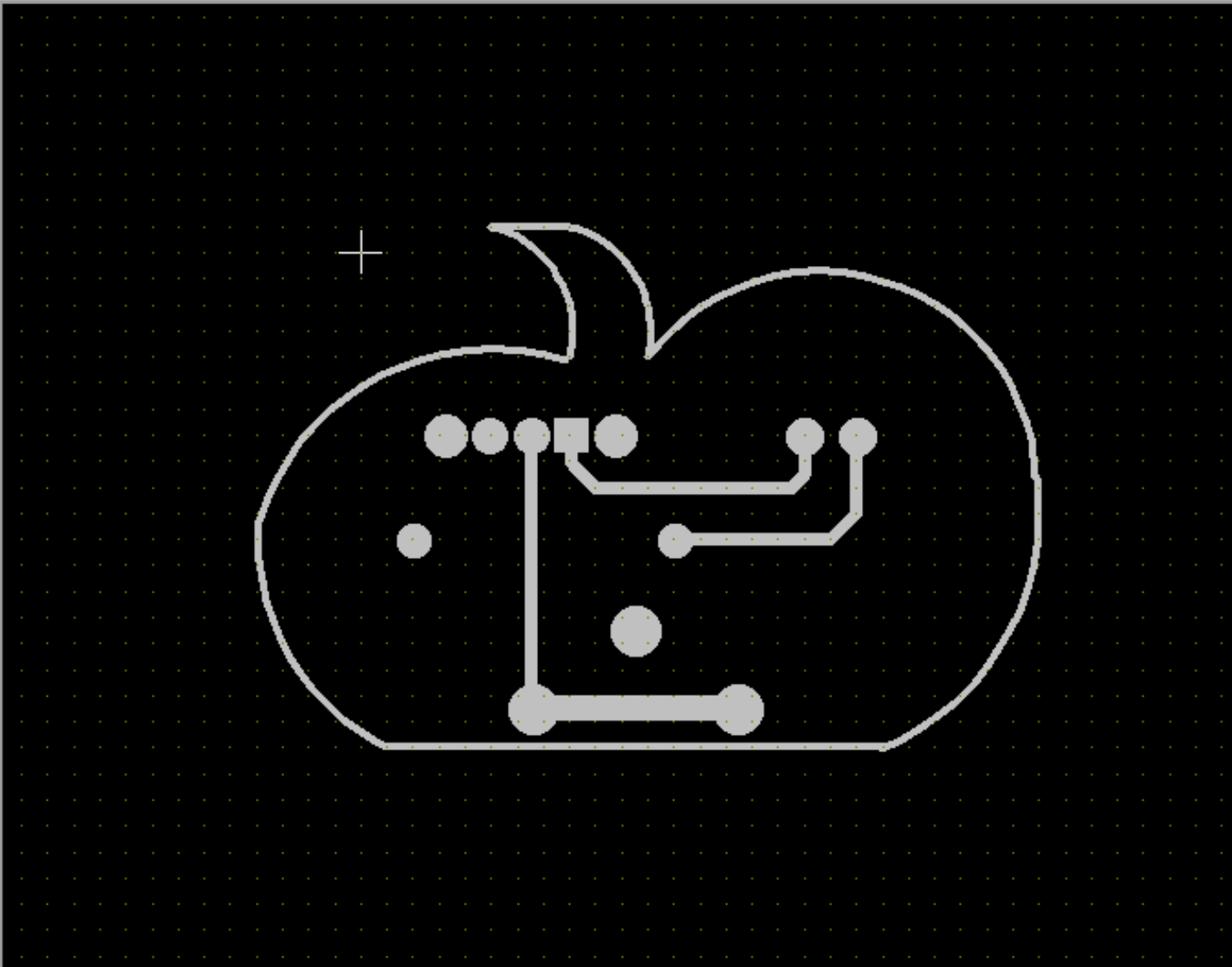
File Preferences Miscellaneous Help



Layer 1

Tool 10

fmt: in X3.4 Y3.4 no LZ

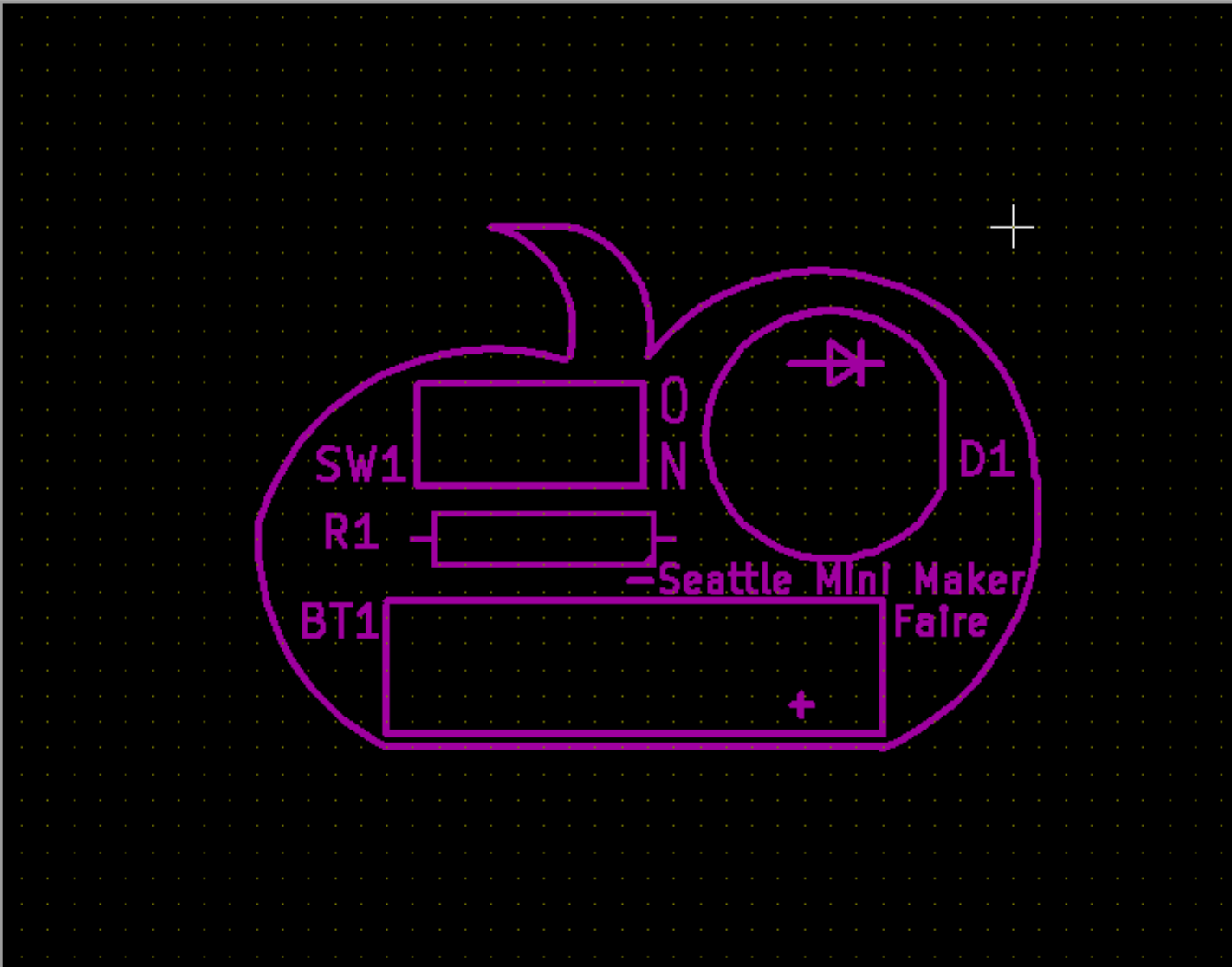


Visibles

- | Layer | Render |
|----------|-------------------------------------|
| Layer 1 | <input type="checkbox"/> |
| Layer 2 | <input type="checkbox"/> |
| Layer 3 | <input checked="" type="checkbox"/> |
| Layer 4 | <input type="checkbox"/> |
| Layer 5 | <input type="checkbox"/> |
| Layer 6 | <input type="checkbox"/> |
| Layer 7 | <input type="checkbox"/> |
| Layer 8 | <input type="checkbox"/> |
| Layer 9 | <input type="checkbox"/> |
| Layer 10 | <input type="checkbox"/> |
| Layer 11 | <input type="checkbox"/> |
| Layer 12 | <input type="checkbox"/> |
| Layer 13 | <input type="checkbox"/> |
| Layer 14 | <input type="checkbox"/> |
| Layer 15 | <input type="checkbox"/> |
| Layer 16 | <input type="checkbox"/> |
| Layer 17 | <input type="checkbox"/> |
| Layer 18 | <input type="checkbox"/> |
| Layer 19 | <input type="checkbox"/> |
| Layer 20 | <input type="checkbox"/> |
| Layer 21 | <input type="checkbox"/> |
| Layer 22 | <input type="checkbox"/> |
| Layer 23 | <input type="checkbox"/> |
| Layer 24 | <input type="checkbox"/> |

Image name	Graphic layer	Img Rot.	Polarity	X Justify	Y Justify	Image Justify Offset
no name	1	0	Normal	Normal	Normal	X=0.000000 Y=0.000000

Image name: "no name" Layer name: "no n..." Z 35 X 6.2000 Y 3.2500 dx 6.2000 dy 3.2500 Inches

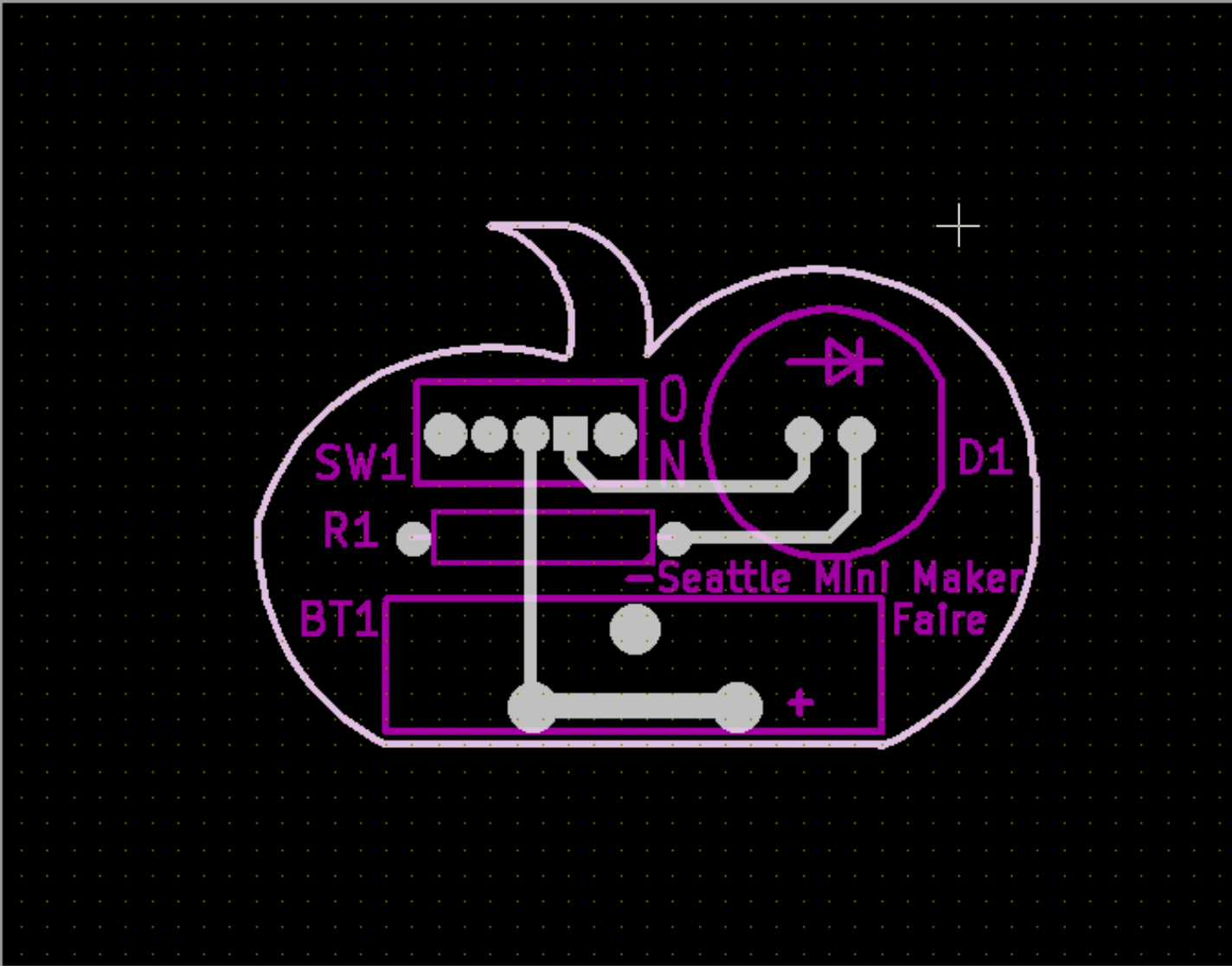


Visibles

Layer	Render
<input checked="" type="checkbox"/> Layer 1	<input type="checkbox"/>
<input type="checkbox"/> Layer 2	<input type="checkbox"/>
<input type="checkbox"/> Layer 3	<input type="checkbox"/>
<input type="checkbox"/> Layer 4	<input type="checkbox"/>
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<input type="checkbox"/> Layer 12	<input type="checkbox"/>
<input type="checkbox"/> Layer 13	<input type="checkbox"/>
<input type="checkbox"/> Layer 14	<input type="checkbox"/>
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<input type="checkbox"/> Layer 16	<input type="checkbox"/>
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<input type="checkbox"/> Layer 19	<input type="checkbox"/>
<input type="checkbox"/> Layer 20	<input type="checkbox"/>
<input type="checkbox"/> Layer 21	<input type="checkbox"/>
<input type="checkbox"/> Layer 22	<input type="checkbox"/>
<input type="checkbox"/> Layer 23	<input type="checkbox"/>
<input type="checkbox"/> Layer 24	<input type="checkbox"/>

Image name	Graphic layer	Img Rot.	Polarity	X Justify	Y Justify	Image Justify Offset
no name	1	0	Normal	Normal	Normal	X=0.000000 Y=0.000000

Image name: "no name" Layer name: "no n..." Z 35 X 7.4500 Y 3.2000 dx 7.4500 dy 3.2000 Inches



Visibles

Layer	Render
<input checked="" type="checkbox"/> Layer 1	<input type="checkbox"/>
<input checked="" type="checkbox"/> Layer 2	<input type="checkbox"/>
<input checked="" type="checkbox"/> Layer 3	<input checked="" type="checkbox"/>
<input checked="" type="checkbox"/> Layer 4	<input type="checkbox"/>
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<input type="checkbox"/> Layer 22	<input type="checkbox"/>
<input type="checkbox"/> Layer 23	<input type="checkbox"/>
<input type="checkbox"/> Layer 24	<input type="checkbox"/>

Image name	Graphic layer	Img Rot.	Polarity	X Justify	Y Justify	Image Justify Offset
no name	1	0	Normal	Normal	Normal	X=0.000000 Y=0.000000

Image name: "no name" Layer name: "no n..." Z 35 X 7.3500 Y 3.2000 dx 7.3500 dy 3.2000 Inches

Create a board with KiCAD

- What is a PCB?
- What is a KiCAD?
- Block diagram
- Schematic
- Schematic attribute editor
- Error check the schematic
- PCB layout
- Error check the layout
- Gerber files
- **Build boards**

PCB price factors:

- complexity - small space/trace or special features
- size of the board and number of boards
- turn around time

PCB Pooling Services

DorkbotPDX PCB http://dorkbotpdx.org/wiki/pcb_order

- Qty=3, two-layer boards: \$5 per square inch
- Today's board example would be ~\$7.50 for qty=3
- Qty=3, four-layer boards: \$10 per square inch
- Purple solder mask
- 2 layer boards ship approx in 14 days
- Prices include shipping

Midnight Maker <http://www.midnightmaker.com/>

- Qty=3, two-layer boards: \$5 per square inch
- Today's board example would be ~\$7.50 for qty=3
- Qty=3, four-layer boards: \$10 per square inch
- Black solder mask
- One week manufacturing time
- Prices include shipping

PCB Service Companies

Sunstone <http://www.sunstone.com/>

- Mulino, OR
- ValueProto service
- Today's example board would cost \$38.50, qty=3
- Available in two weeks or less includes shipping
- Also have more options for faster turn around time

Seed Studio

<http://www.seeedstudio.com/>

- Fusion PCB service
- \$9.90 for 10 boards up to 5cm X 5cm in size
- Today's example board would cost \$9.90, Qty=10
- Plus shipping \$4.10 to ship to the State of Washington
- Shipping 10-30 to the US

PCB samples thanks to:
DorkbotPDX PCB
Midnight Maker
Seed Studio

Eric Thompson
LowVoltageLabs.com

